

# Kolar-1 SVT Logic Schematics

KL1KR-1  
VER 4.02  
Nov/1/2017

BASE LOGIC :  
kolar\_sit-r\_lcfc\_20171026

- 1.TITLE PAGE

2.EC HISTORY

3.CPU(1/16) : DDI/EDP

4.CPU(2/16) : DDR CHANNEL-A

5.CPU(3/16) : DDR CHANNEL-B

6.CPU(4/16) : MISC/JTAG

7.CPU(5/16) : LPC/SPI/SMBUS/C-LINK

8.CPU(6/16) : LPSS/ISH

9.CPU(7/16) : AUDIO/SDXC

10.CPU(8/16) : PCIE/USB/SATA

11.CPU(9/16) : CSI-2/EMMC

12.CPU(10/16) : CLOCK SIGNALS

13.CPU(11/16) : SYSTEM PM

14.CPU(12/16) : CPU POWER (1/2)

15.CPU(13/16) : CPU POWER (2/2)

16.CPU(14/16) : PCH POWER

17.CPU(15/16) : GND

18.CPU(16/16) : CFG/RESERVED

19.XDP CONNECTOR

20.RTC BATTERY

21.SPI FLASH

22.DDR4 BASE MEMORY CH-A (1/2)

23.DDR4 BASE MEMORY CH-A (2/2)

24.DDR4 SO DIMM CHANNEL-B (1/2)

25.DDR4 SO DIMM CHANNEL-B (2/2)

26.LCD I/F

27.LID/MIC/CAMERA/PWR SW

28.DDI DEMUX/HDMI LEVEL SHIFTER

29.USB TYPE-C SWITCH

30.BLANK

31.ALPINE RIDGE(1/2)

32.ALPINE RIDGE(2/2)

33.POWER DELIVERY (SN1701012RSLR)

34.TYPE-C LOW LOGIC MUX

35.CS18 SIDE DOCKING CONNECTOR

36.USB TYPE-C CONNECTOR
- 37.HDMI CONNECTOR

38.M.2 SOCKET 3 MODULE I/F

39.USB POWER/CONN

40.BLANK

41.GBE JACKSONVILLE

42.GBE LAN SWITCH

43.GBE MAGNETICS

44.RJ45 CONNECTOR

45.M.2 SOCKET 1 MODULE I/F

46.M.2 SOCKET 2 MODULE I/F

47.MEDIA CARD/AUDIO CONNECTOR

48.N17S-LG(1/6) PEG I/F

49.N17S-LG(2/6) VRAM I/F

50.N17S-LG(3/6) POWER

51.N17S-LG(4/6) POWER 2

52.N17S-LG(5/6) GND

53.N17S-LG(6/6) GPIO / XTAL

54.VRAM CHANNEL-A

55.MEC1663 (1/3)

56.MEC1663 (2/3)

57.MEC1663 (3/3)

58.KEYBOARD/TRACK POINT

59.TOUCH PAD/NFC

60.SCR/FPR/LED

61.FAN CONNECTOR

62.APS G-SENSOR

63.DISCRETE TPM 2.0

64.SMBUS SWITCH/LPC DEBUG PORT

65.THINK ENGINE-3 (1/2)

66.THINK ENGINE-3 (2/2)

67.AUDIO ALC3287-CG

68.AUDIO JACK & EXT MIC I/F

69.AUDIO SPEAKER I/F

70.DC-IN

71.BLANK
- 72.BATTERY INPUT

73.BATTERY CHARGER (BQ25700)

74.DC/DC VCC5M/VCC3M (TPS51285B-1)

75.DC/DC IMVP8 CONTROLLER (NCP81218)

76.DC/DC VCCCPUCORE (NCP302045)

77.DC/DC VCCGFXCORE\_I (NCP302045)

78.DC/DC VCCSA (NCP302035)

79.U22 UNIQUE

80.BLANK

81.DC/DC VCC1R0\_SUS (NB693GQ)

82.LOAD SW VCCST & VCCSTG

83.DC/DC VCC1R2A /0R6B/2R5A (NB687)

84.BLANK

85.BLANK

86.DC/DC VCC1R8\_SUS (BU90104GWZ)

87.BLANK

88.DC/DC NVDD (NCP81278)

89.DC/DC VCC1R35VIDEO (NB693GQ-Z)

90.VCC1R0VIDEO (BD9B304QWZ)

91.VCC1R8VIDEO\_AON (BD9B304QWZ)

92.SW VCC1R8VIDEO\_MAIN

93.LOAD SW SUS

94.LOAD SW LAN

95.LOAD SW B

96.LOAD SW WLAN

97.PTH FOR SCREW HOLES

EC HISTORY

CS18 KL1KR-1  
(kolar\_sit-r\_lcfc\_20171026)

VER.4.01 10/30/2017 APPLIED HW\_ECR001-002 / PWR\_ECR001  
VER.4.02 11/1/2017 APPLIED HW\_ECR003-004 / SIT-R HW\_ECR011

TABLE: Chip Capacitor Thermal Characteristics

		Code
-55 to 150degC -55 to 125degC	+/-30ppm/degC +/-30ppm/degC	NPO C0G
-55 to 125degC -55 to 105degC -55 to 85degC	+/-15% +/-22% +/-15%	X7R X6S X5R

TABLE: Chip Capacitor Tolerance

Tolerance	Code
+/-0.25pF +/-0.5pF	C D
+/-5% +/-10% +/-20% +80/-20%	J K M Z

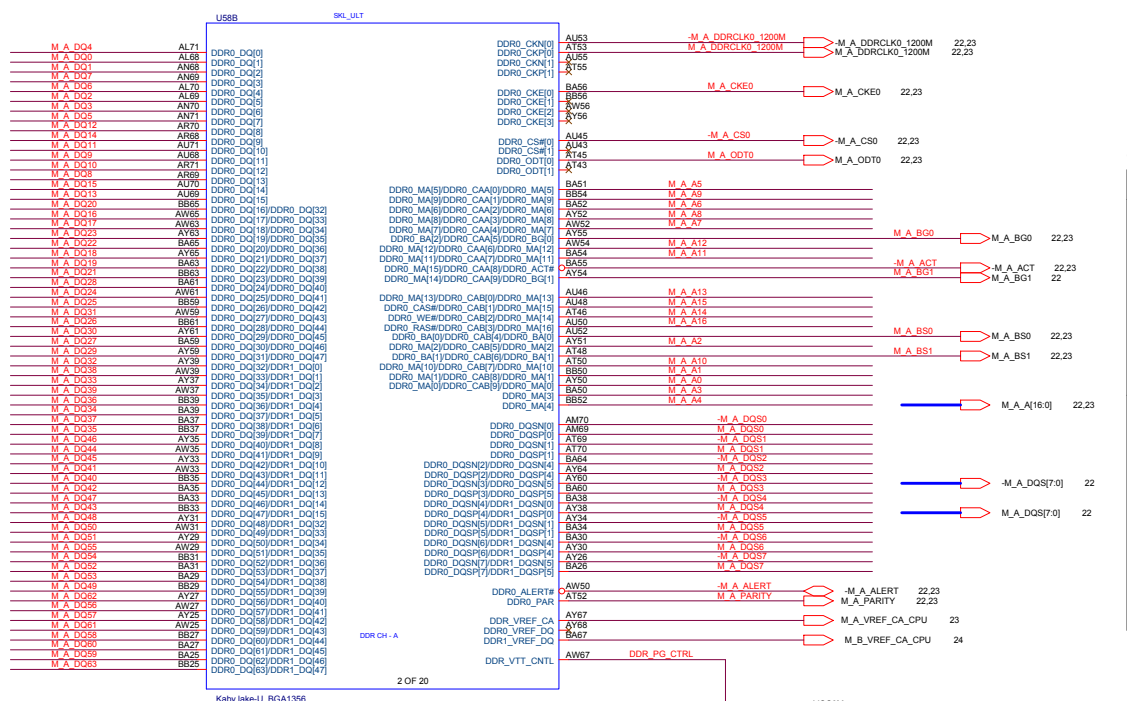
TABLE: Chip Part Dimension

Size [mm]	mm Size Code	Inch Size Code
0.40 x 0.20 0.60 x 0.30 1.00 x 0.50 1.60 x 0.80 2.00 x 1.25 2.00 x 1.60 2.50 x 2.00 3.20 x 1.60 3.20 x 2.50 4.50 x 1.60 4.50 x 2.50 4.50 x 3.20 5.00 x 2.50 6.40 x 3.20	0402 0603 1005 1608 2125 2016 2520 3216 3225 4516 4525 4532 5025 6432	01005 0201 0402 0603 0805 0806 1008 1206 1210 1806 1810 1812 2010 2512

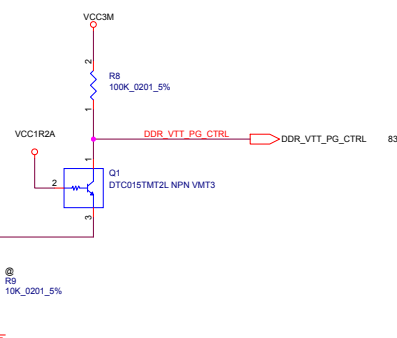
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LOGIC



	Pin	Interleave	Non-Interleave
Block 0	AL71	DDR0_DQ[0]	DDR0_DQ[0]
	AL68	DDR0_DQ[1]	DDR0_DQ[1]
	AN68	DDR0_DQ[2]	DDR0_DQ[2]
	AN69	DDR0_DQ[3]	DDR0_DQ[3]
	AL70	DDR0_DQ[4]	DDR0_DQ[4]
	AL69	DDR0_DQ[5]	DDR0_DQ[5]
	AN70	DDR0_DQ[6]	DDR0_DQ[6]
	AN71	DDR0_DQ[7]	DDR0_DQ[7]
	AR70	DDR0_DQ[8]	DDR0_DQ[8]
	AR68	DDR0_DQ[9]	DDR0_DQ[9]
	AU71	DDR0_DQ[10]	DDR0_DQ[10]
	AU68	DDR0_DQ[11]	DDR0_DQ[11]
AR71	DDR0_DQ[12]	DDR0_DQ[12]	
AR69	DDR0_DQ[13]	DDR0_DQ[13]	
AU70	DDR0_DQ[14]	DDR0_DQ[14]	
AU69	DDR0_DQ[15]	DDR0_DQ[15]	
Block 2	BB65	DDR0_DQ[16]	DDR0_DQ[32]
	AW65	DDR0_DQ[17]	DDR0_DQ[33]
	AW63	DDR0_DQ[18]	DDR0_DQ[34]
	AY63	DDR0_DQ[19]	DDR0_DQ[35]
	BA65	DDR0_DQ[20]	DDR0_DQ[36]
	AY65	DDR0_DQ[21]	DDR0_DQ[37]
	BA63	DDR0_DQ[22]	DDR0_DQ[38]
	BB63	DDR0_DQ[23]	DDR0_DQ[39]
	BA61	DDR0_DQ[24]	DDR0_DQ[40]
	AW61	DDR0_DQ[25]	DDR0_DQ[41]
	BB59	DDR0_DQ[26]	DDR0_DQ[42]
	AW59	DDR0_DQ[27]	DDR0_DQ[43]
BB61	DDR0_DQ[28]	DDR0_DQ[44]	
AY61	DDR0_DQ[29]	DDR0_DQ[45]	
BA59	DDR0_DQ[30]	DDR0_DQ[46]	
AY59	DDR0_DQ[31]	DDR0_DQ[47]	
Block 4	AY39	DDR0_DQ[32]	DDR1_DQ[0]
	AW39	DDR0_DQ[33]	DDR1_DQ[1]
	AY37	DDR0_DQ[34]	DDR1_DQ[2]
	AW37	DDR0_DQ[35]	DDR1_DQ[3]
	BB39	DDR0_DQ[36]	DDR1_DQ[4]
	BA39	DDR0_DQ[37]	DDR1_DQ[5]
	BA37	DDR0_DQ[38]	DDR1_DQ[6]
	BB37	DDR0_DQ[39]	DDR1_DQ[7]
	AY35	DDR0_DQ[40]	DDR1_DQ[8]
	AW35	DDR0_DQ[41]	DDR1_DQ[9]
	AY33	DDR0_DQ[42]	DDR1_DQ[10]
	AW33	DDR0_DQ[43]	DDR1_DQ[11]
BB35	DDR0_DQ[44]	DDR1_DQ[12]	
BA35	DDR0_DQ[45]	DDR1_DQ[13]	
BA33	DDR0_DQ[46]	DDR1_DQ[14]	
BB33	DDR0_DQ[47]	DDR1_DQ[15]	
Block 6	AY31	DDR0_DQ[48]	DDR1_DQ[32]
	AW31	DDR0_DQ[49]	DDR1_DQ[33]
	AY29	DDR0_DQ[50]	DDR1_DQ[34]
	AW29	DDR0_DQ[51]	DDR1_DQ[35]
	BB31	DDR0_DQ[52]	DDR1_DQ[36]
	BA31	DDR0_DQ[53]	DDR1_DQ[37]
	BA29	DDR0_DQ[54]	DDR1_DQ[38]
	BB29	DDR0_DQ[55]	DDR1_DQ[39]
	AY27	DDR0_DQ[56]	DDR1_DQ[40]
	AW27	DDR0_DQ[57]	DDR1_DQ[41]
	AY25	DDR0_DQ[58]	DDR1_DQ[42]
	AW25	DDR0_DQ[59]	DDR1_DQ[43]
BB27	DDR0_DQ[60]	DDR1_DQ[44]	
BA27	DDR0_DQ[61]	DDR1_DQ[45]	
BA25	DDR0_DQ[62]	DDR1_DQ[46]	
BB25	DDR0_DQ[63]	DDR1_DQ[47]	



	Pin	Interleave	Non-Interleave
Block 0	AM70	DDR0_QQSN[0]	DDR0_QQSN[0]
	AM69	DDR0_QQSP[0]	DDR0_QQSP[0]
	AT69	DDR0_QQSN[1]	DDR0_QQSN[1]
	AT70	DDR0_QQSP[1]	DDR0_QQSP[1]
Block 2	BA64	DDR0_QQSN[2]	DDR0_QQSN[4]
	AY64	DDR0_QQSP[2]	DDR0_QQSP[4]
	AY60	DDR0_QQSN[3]	DDR0_QQSN[5]
	BA60	DDR0_QQSP[3]	DDR0_QQSP[5]
Block 4	BA38	DDR0_QQSN[4]	DDR1_QQSN[0]
	AY38	DDR0_QQSP[4]	DDR1_QQSP[0]
	AY34	DDR0_QQSN[5]	DDR1_QQSN[1]
	BA34	DDR0_QQSP[5]	DDR1_QQSP[1]
Block 6	BA30	DDR0_QQSN[6]	DDR1_QQSN[4]
	AY30	DDR0_QQSP[6]	DDR1_QQSP[4]
	AY26	DDR0_QQSN[7]	DDR1_QQSN[5]
	BA26	DDR0_QQSP[7]	DDR1_QQSP[5]



Pin	DDR3L	LPDDR3	DDR4
BA51	DDR0_MA[5]	DDR0_CAA[0]	DDR0_MA[5]
BB54	DDR0_MA[9]	DDR0_CAA[1]	DDR0_MA[9]
BA52	DDR0_MA[6]	DDR0_CAA[2]	DDR0_MA[6]
AY52	DDR0_MA[8]	DDR0_CAA[3]	DDR0_MA[8]
AW52	DDR0_MA[7]	DDR0_CAA[4]	DDR0_MA[7]
AY55	DDR0_BA[2]	DDR0_CAA[5]	DDR0_BG[0]
AW54	DDR0_MA[12]	DDR0_CAA[6]	DDR0_MA[12]
BA54	DDR0_MA[11]	DDR0_CAA[7]	DDR0_MA[11]
BA55	DDR0_MA[15]	DDR0_CAA[8]	DDR0_ACT#
AY54	DDR0_MA[14]	DDR0_CAA[9]	DDR0_BG[1]
AU46	DDR0_MA[13]	DDR0_CAB[0]	DDR0_MA[13]
AU48	DDR0_CAS#	DDR0_CAB[1]	DDR0_MA[15]
AT46	DDR0_WE#	DDR0_CAB[2]	DDR0_MA[14]
AU50	DDR0_RAS#	DDR0_CAB[3]	DDR0_MA[16]
AU52	DDR0_BA[0]	DDR0_CAB[4]	DDR0_BA[0]
AY51	DDR0_MA[2]	DDR0_CAB[5]	DDR0_MA[2]
AT48	DDR0_BA[1]	DDR0_CAB[6]	DDR0_BA[1]
AT50	DDR0_MA[10]	DDR0_CAB[7]	DDR0_MA[10]
BB50	DDR0_MA[1]	DDR0_CAB[8]	DDR0_MA[1]
AY50	DDR0_MA[0]	DDR0_CAB[9]	DDR0_MA[0]
BA50	DDR0_MA[3]	Not Used	DDR0_MA[3]
BB52	DDR0_MA[4]	Not Used	DDR0_MA[4]

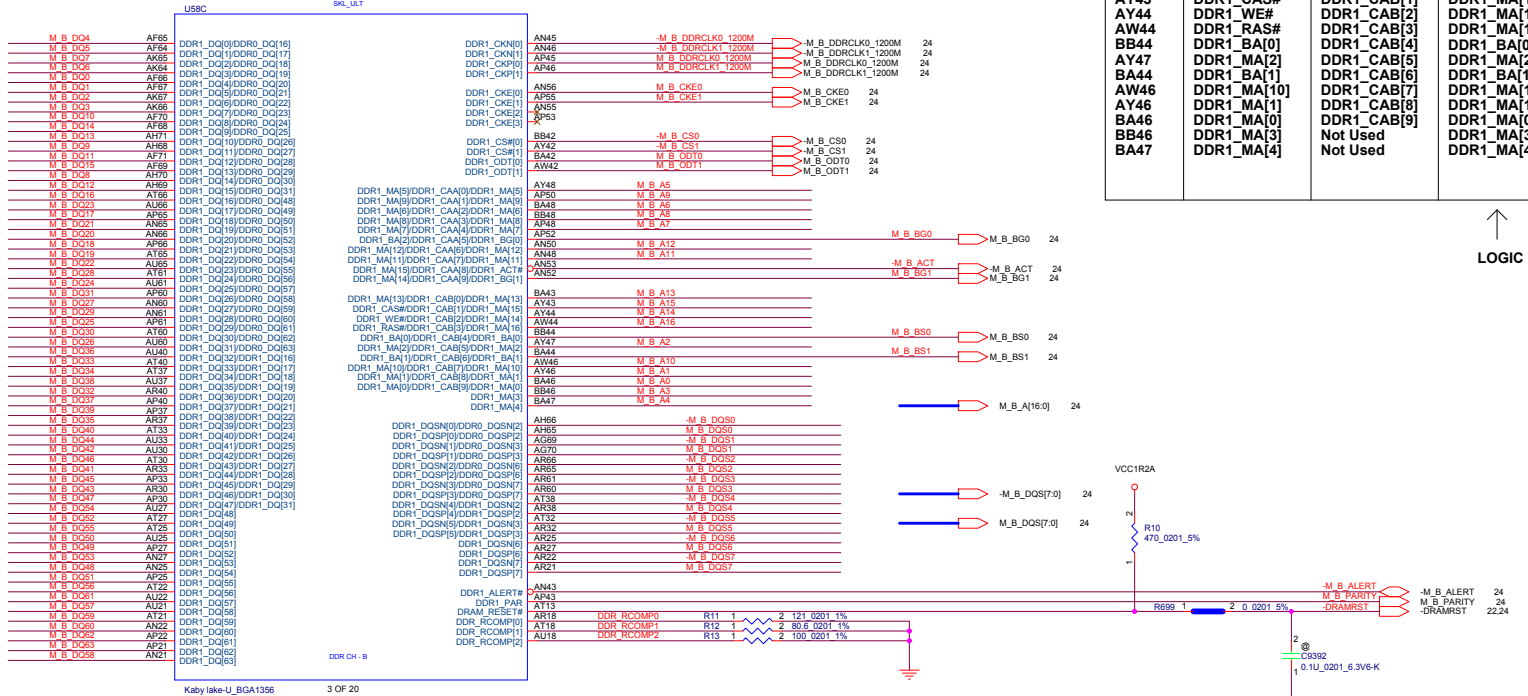
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TABLE

	Pin	Interleave	Non-Interleave
Block 1	AF65	DDR1_DQ[0]	DDR0_DQ[16]
	AF64	DDR1_DQ[1]	DDR0_DQ[17]
	AK65	DDR1_DQ[2]	DDR0_DQ[18]
	AK64	DDR1_DQ[3]	DDR0_DQ[19]
	AF66	DDR1_DQ[4]	DDR0_DQ[20]
	AF67	DDR1_DQ[5]	DDR0_DQ[21]
	AK67	DDR1_DQ[6]	DDR0_DQ[22]
	AK66	DDR1_DQ[7]	DDR0_DQ[23]
	AF70	DDR1_DQ[8]	DDR0_DQ[24]
	AF68	DDR1_DQ[9]	DDR0_DQ[25]
	AH71	DDR1_DQ[10]	DDR0_DQ[26]
	AH68	DDR1_DQ[11]	DDR0_DQ[27]
	AF71	DDR1_DQ[12]	DDR0_DQ[28]
	AF69	DDR1_DQ[13]	DDR0_DQ[29]
	AH70	DDR1_DQ[14]	DDR0_DQ[30]
	AH69	DDR1_DQ[15]	DDR0_DQ[31]
Block 3	AT66	DDR1_DQ[16]	DDR0_DQ[48]
	AU66	DDR1_DQ[17]	DDR0_DQ[49]
	AP65	DDR1_DQ[18]	DDR0_DQ[50]
	AN65	DDR1_DQ[19]	DDR0_DQ[51]
	AN66	DDR1_DQ[20]	DDR0_DQ[52]
	AP66	DDR1_DQ[21]	DDR0_DQ[53]
	AT65	DDR1_DQ[22]	DDR0_DQ[54]
	AU65	DDR1_DQ[23]	DDR0_DQ[55]
	AT61	DDR1_DQ[24]	DDR0_DQ[56]
	AU61	DDR1_DQ[25]	DDR0_DQ[57]
	AP60	DDR1_DQ[26]	DDR0_DQ[58]
	AN60	DDR1_DQ[27]	DDR0_DQ[59]
	AN61	DDR1_DQ[28]	DDR0_DQ[60]
	AP61	DDR1_DQ[29]	DDR0_DQ[61]
	AT60	DDR1_DQ[30]	DDR0_DQ[62]
	AU60	DDR1_DQ[31]	DDR0_DQ[63]
Block 5	AU40	DDR1_DQ[32]	DDR1_DQ[16]
	AT40	DDR1_DQ[33]	DDR1_DQ[17]
	AT37	DDR1_DQ[34]	DDR1_DQ[18]
	AU37	DDR1_DQ[35]	DDR1_DQ[19]
	AR40	DDR1_DQ[36]	DDR1_DQ[20]
	AP37	DDR1_DQ[37]	DDR1_DQ[21]
	AR37	DDR1_DQ[38]	DDR1_DQ[22]
	AT33	DDR1_DQ[39]	DDR1_DQ[23]
	AU33	DDR1_DQ[40]	DDR1_DQ[24]
	AU30	DDR1_DQ[41]	DDR1_DQ[25]
	AT30	DDR1_DQ[42]	DDR1_DQ[26]
	AR33	DDR1_DQ[43]	DDR1_DQ[27]
	AP33	DDR1_DQ[44]	DDR1_DQ[28]
	AR30	DDR1_DQ[45]	DDR1_DQ[29]
	AP30	DDR1_DQ[46]	DDR1_DQ[30]
	AP30	DDR1_DQ[47]	DDR1_DQ[31]
Block 7	AU27	DDR1_DQ[48]	DDR1_DQ[48]
	AT27	DDR1_DQ[49]	DDR1_DQ[49]
	AT25	DDR1_DQ[50]	DDR1_DQ[50]
	AU25	DDR1_DQ[51]	DDR1_DQ[51]
	AP27	DDR1_DQ[52]	DDR1_DQ[52]
	AN27	DDR1_DQ[53]	DDR1_DQ[53]
	AN25	DDR1_DQ[54]	DDR1_DQ[54]
	AP25	DDR1_DQ[55]	DDR1_DQ[55]
	AT22	DDR1_DQ[56]	DDR1_DQ[56]
	AU22	DDR1_DQ[57]	DDR1_DQ[57]
	AU21	DDR1_DQ[58]	DDR1_DQ[58]
	AT21	DDR1_DQ[59]	DDR1_DQ[59]
	AN22	DDR1_DQ[60]	DDR1_DQ[60]
	AP22	DDR1_DQ[61]	DDR1_DQ[61]
	AP21	DDR1_DQ[62]	DDR1_DQ[62]
	AN21	DDR1_DQ[63]	DDR1_DQ[63]

LOGIC

LOGIC



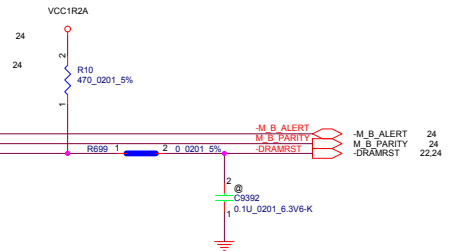
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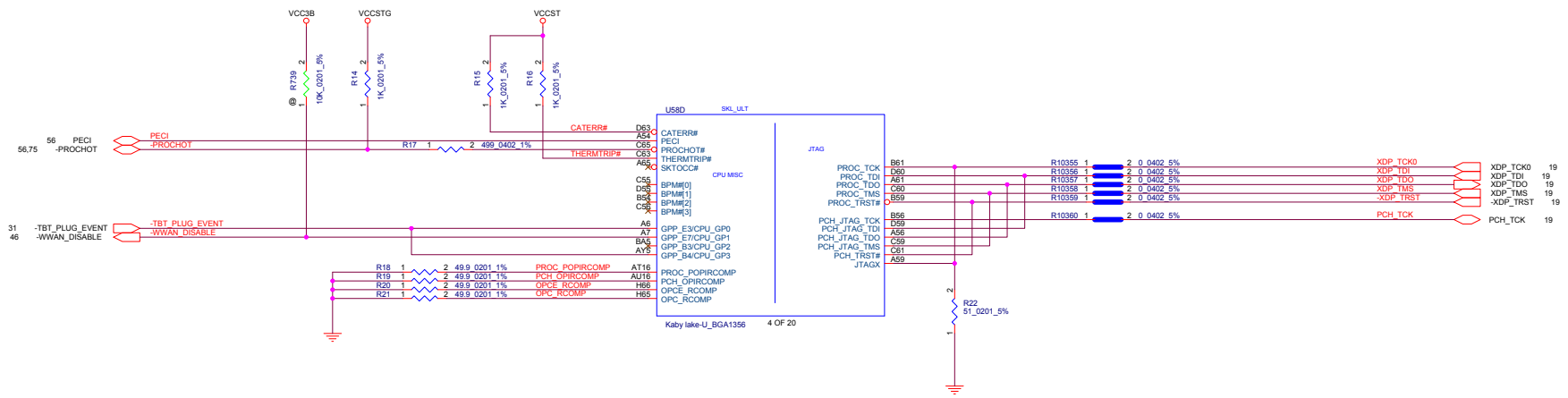
	Pin	Interleave	Non-Interleave
Block 1	AH66	DDR1_DQSN[0]	DDR0_DQSN[2]
	AH65	DDR1_DQSP[0]	DDR0_DQSP[2]
	AG69	DDR1_DQSN[1]	DDR0_DQSN[3]
	AG70	DDR1_DQSP[1]	DDR0_DQSP[3]
Block 3	AR66	DDR1_DQSN[2]	DDR0_DQSN[6]
	AR65	DDR1_DQSP[2]	DDR0_DQSP[6]
	AR61	DDR1_DQSN[3]	DDR0_DQSN[7]
	AR60	DDR1_DQSP[3]	DDR0_DQSP[7]
Block 5	AT38	DDR1_DQSN[4]	DDR1_DQSN[2]
	AR38	DDR1_DQSP[4]	DDR1_DQSP[2]
	AT32	DDR1_DQSN[5]	DDR1_DQSN[3]
	AR32	DDR1_DQSP[5]	DDR1_DQSP[3]
Block 7	AR25	DDR1_DQSN[6]	DDR1_DQSN[6]
	AR27	DDR1_DQSP[6]	DDR1_DQSP[6]
	AR22	DDR1_DQSN[7]	DDR1_DQSN[7]
	AR21	DDR1_DQSP[7]	DDR1_DQSP[7]

TABLE

Pin	DDR3L	LPDDR3	DDR4
AY48	DDR1_MA[5]	DDR1_CAA[0]	DDR1_MA[5]
AP50	DDR1_MA[9]	DDR1_CAA[1]	DDR1_MA[9]
BA48	DDR1_MA[6]	DDR1_CAA[2]	DDR1_MA[6]
BB48	DDR1_MA[8]	DDR1_CAA[3]	DDR1_MA[8]
AP48	DDR1_MA[7]	DDR1_CAA[4]	DDR1_MA[7]
AP52	DDR1_BA[2]	DDR1_CAA[5]	DDR1_BG[0]
AN50	DDR1_MA[12]	DDR1_CAA[6]	DDR1_MA[12]
AN48	DDR1_MA[11]	DDR1_CAA[7]	DDR1_MA[11]
AN53	DDR1_MA[16]	DDR1_CAA[8]	DDR1_ACT#
AN52	DDR1_MA[14]	DDR1_CAA[9]	DDR1_BG[1]
BA43	DDR1_MA[13]	DDR1_CAB[0]	DDR1_MA[13]
AY43	DDR1_CAS#	DDR1_CAB[1]	DDR1_MA[15]
AY44	DDR1_WE#	DDR1_CAB[2]	DDR1_MA[14]
AW44	DDR1_RAS#	DDR1_CAB[3]	DDR1_MA[16]
BB44	DDR1_BA[0]	DDR1_CAB[4]	DDR1_BA[0]
AY47	DDR1_BA[1]	DDR1_CAB[5]	DDR1_MA[2]
BA44	DDR1_BA[2]	DDR1_CAB[6]	DDR1_BA[1]
AW46	DDR1_MA[10]	DDR1_CAB[7]	DDR1_MA[10]
AY46	DDR1_MA[11]	DDR1_CAB[8]	DDR1_MA[11]
BA46	DDR1_MA[0]	DDR1_CAB[9]	DDR1_MA[0]
BB46	DDR1_MA[3]	Not Used	DDR1_MA[3]
BA47	DDR1_MA[4]	Not Used	DDR1_MA[4]

LOGIC





SPI0_MOSI (Boot Halt)	
HIGH	Disabled (Default)
LOW	Enabled

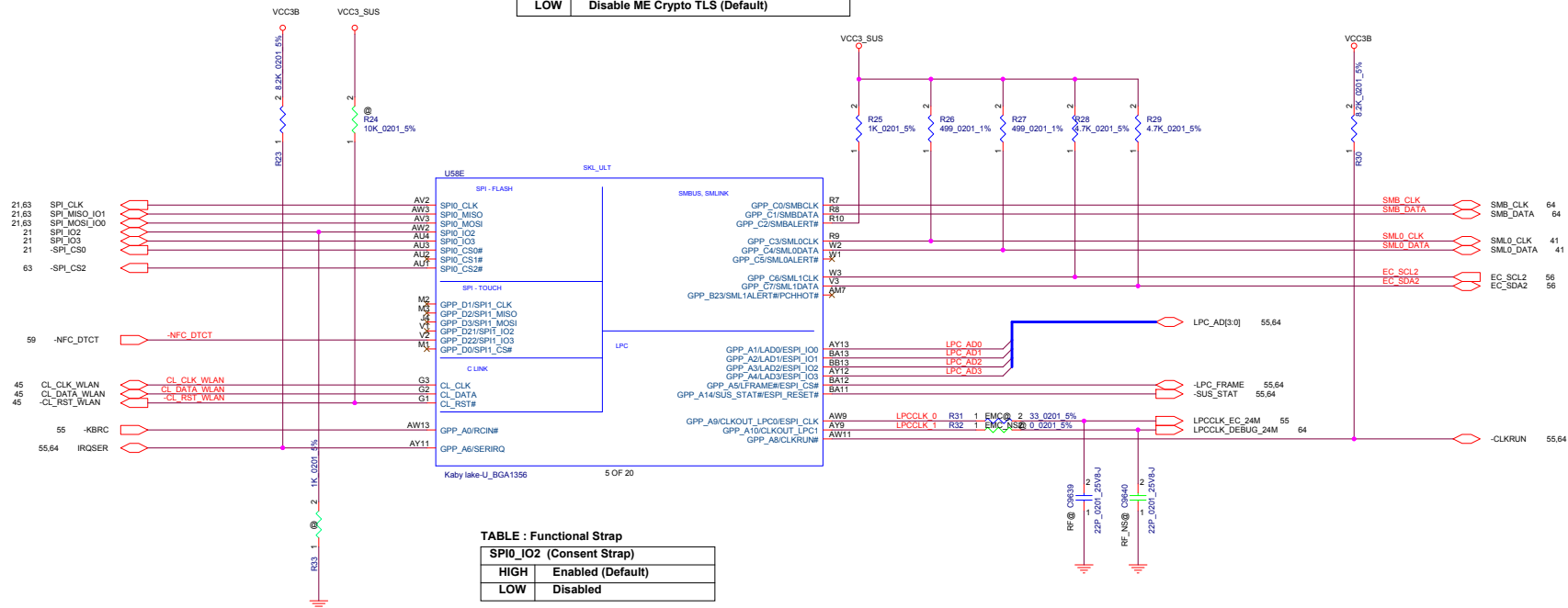
SPI0_MISO (JTAG ODT Disable)	
HIGH	Enabled (Default)
LOW	Disabled

GPP_C5/SML0ALERT # (LPC or eSPI)	
HIGH	eSPI is selected
LOW	LPC is selected (Default)

← LOGIC

GPP_C2/SMBALERT# (TLS Confidentiality)	
HIGH	Enable ME Crypto TLS with Confidentiality
LOW	Disable ME Crypto TLS (Default)

← LOGIC

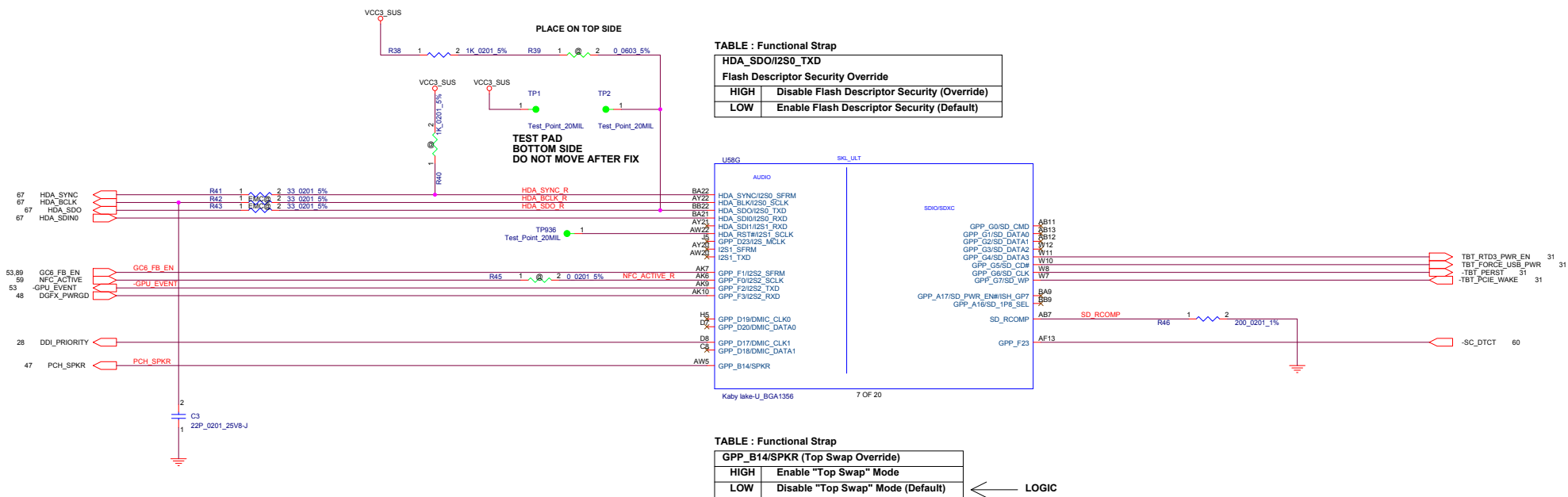


SPI0_IO2 (Consent Strap)	
HIGH	Enabled (Default)
LOW	Disabled

SPI0_IO3 (A0 Personality Strap)	
HIGH	Disabled (Default)
LOW	Enabled



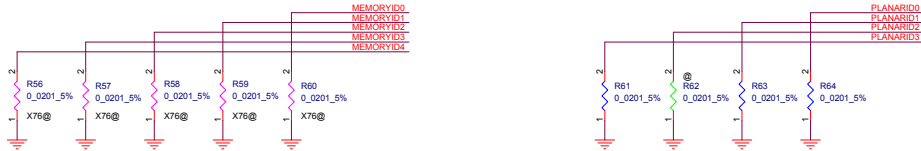






TABLE

MEMORYID[4..0]	U125, U126, U127, U128			
00000b	Micron	MT40A512M16HA-083E:A	8Gbit SDP	4GB (2133)
00001b	Micron	MT40A1G16HBA-083E:A	16Gbit DDP	8GB (2133)
00010b	Samsung	K4A8G16SWB-BCPB	8Gbit SDP	4GB (2133)
00011b	SK Hynix	T.B.D.		
00100b	SK Hynix	T.B.D.		
01000b	Micron	MT40A512M16JY-083E:B	8Gbit SDP	4GB (2400)
01001b	Micron	MT40A1G16WBU-083E:B	16Gbit DDP	8GB (2400)
01010b	Samsung	K4A8G16SWC-BCRC	8Gbit SDP	4GB (2400)
01011b	Samsung	K4AAG16SWB-MCRC	16Gbit DDP	8GB (2400)
01100b	SK Hynix	H5AN8G6NAFR-UHC	8Gbit SDP	4GB (2400)
01101b	SK Hynix	H5ANAG6NAMR-UHC	16Gbit DDP	8GB (2400)
0110b	Micron	MT40A512M16LY-075:E	8Gbit SDP	4GB (2400)
11111b	NO_ASM		No Soldered Memory	

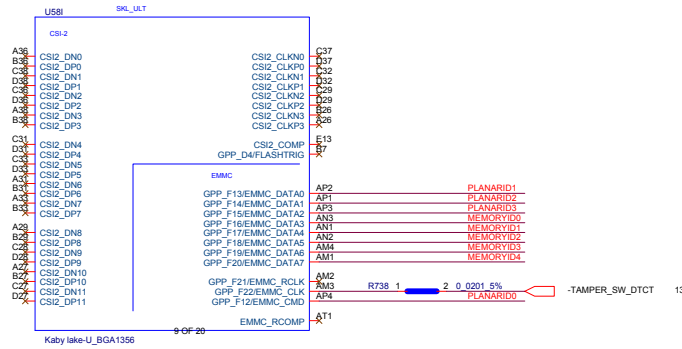


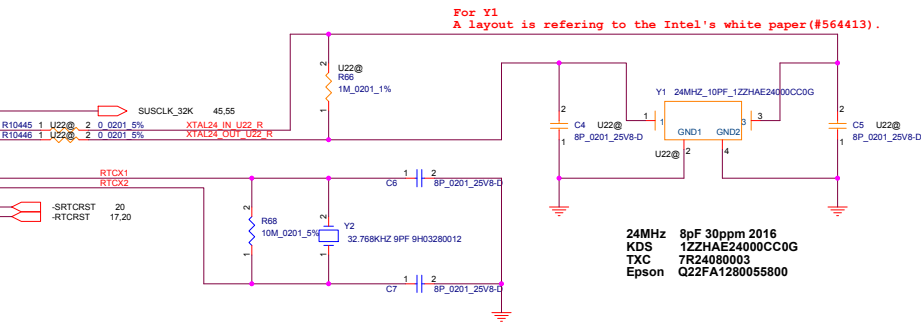
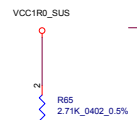
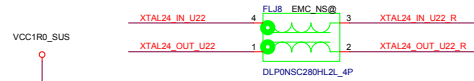
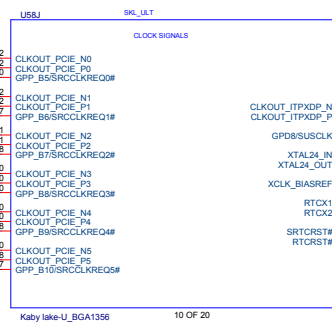
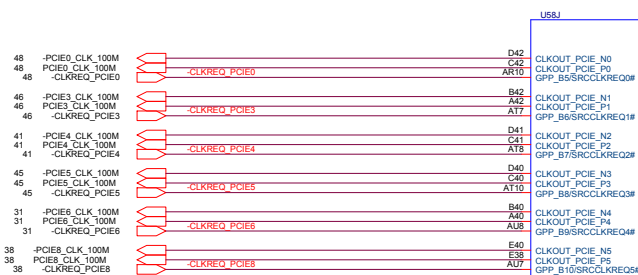
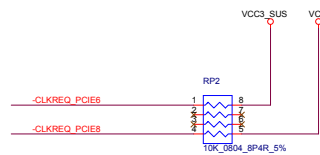
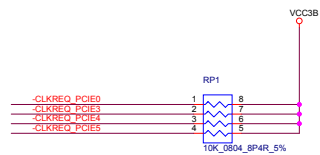
TABLE

LEVEL	PLANAR ID			
	3	2	1	0
1	NA	NA	NA	NA
0	ASM	ASM	ASM	ASM

TABLE

LEVEL	PLANARID[3..0]
EVT	0000B
FVT	0001B
SIT	0010B
SIT-R	0011B
SVT	0100B

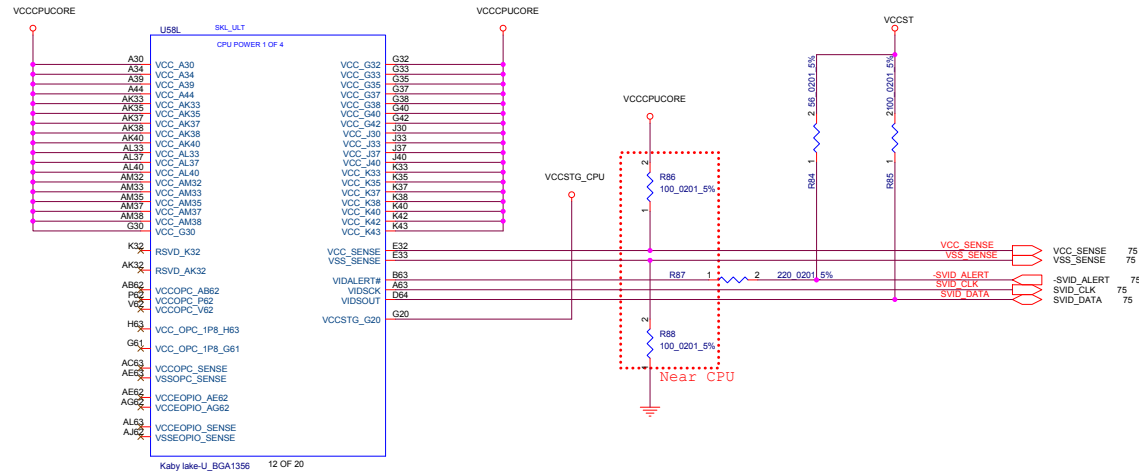
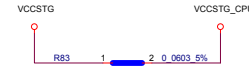
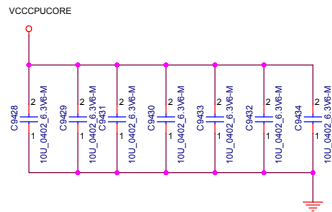
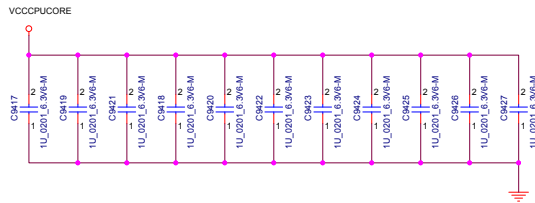
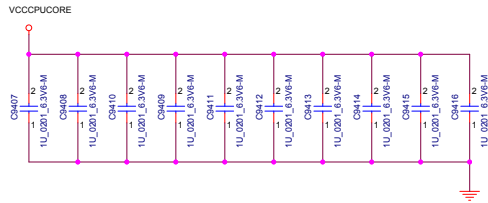
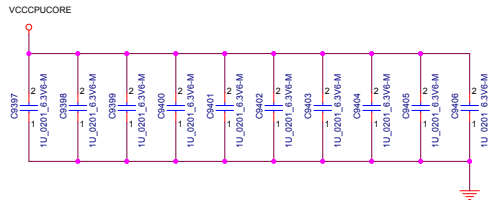




32.768kHz 9pF 20ppm 3215  
 TXC 9H03280012  
 KDS 1TJF090DJ1A000B  
 EPSON X1A000141000200

24MHz 8pF 30ppm 2016  
 KDS 1ZZHAE24000CC0G  
 TXC 7R24080003  
 Epson Q22FA1280055800





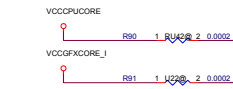
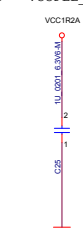
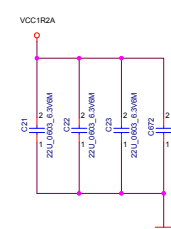
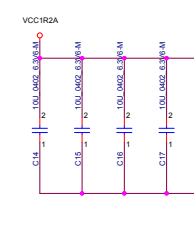
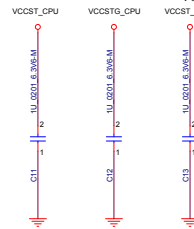
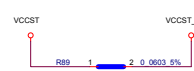
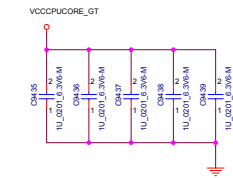
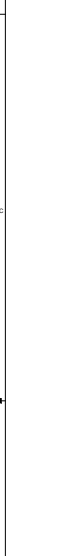
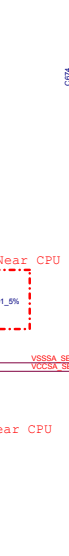
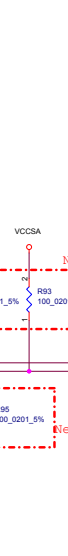
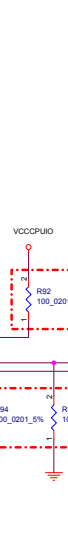
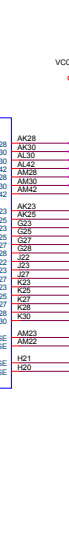
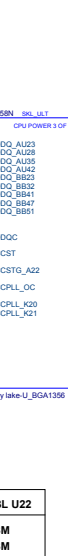
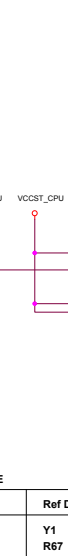
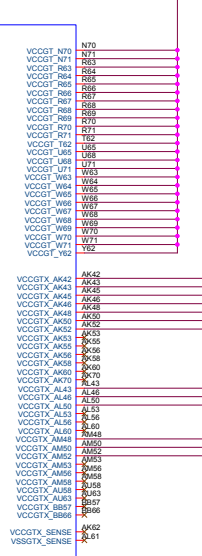
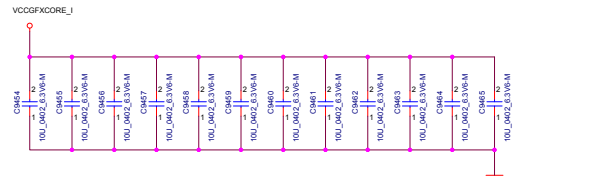
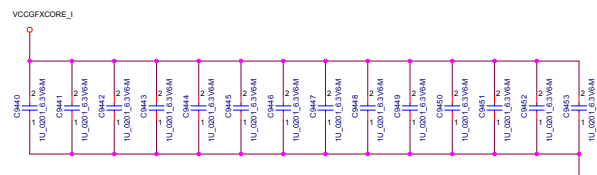
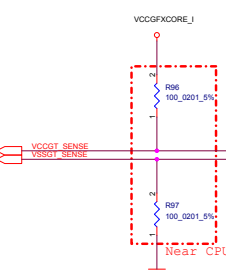
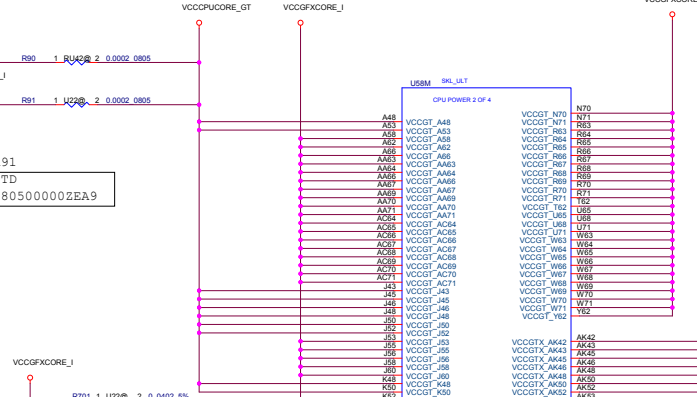
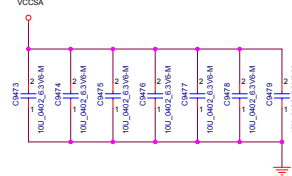
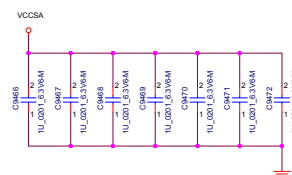


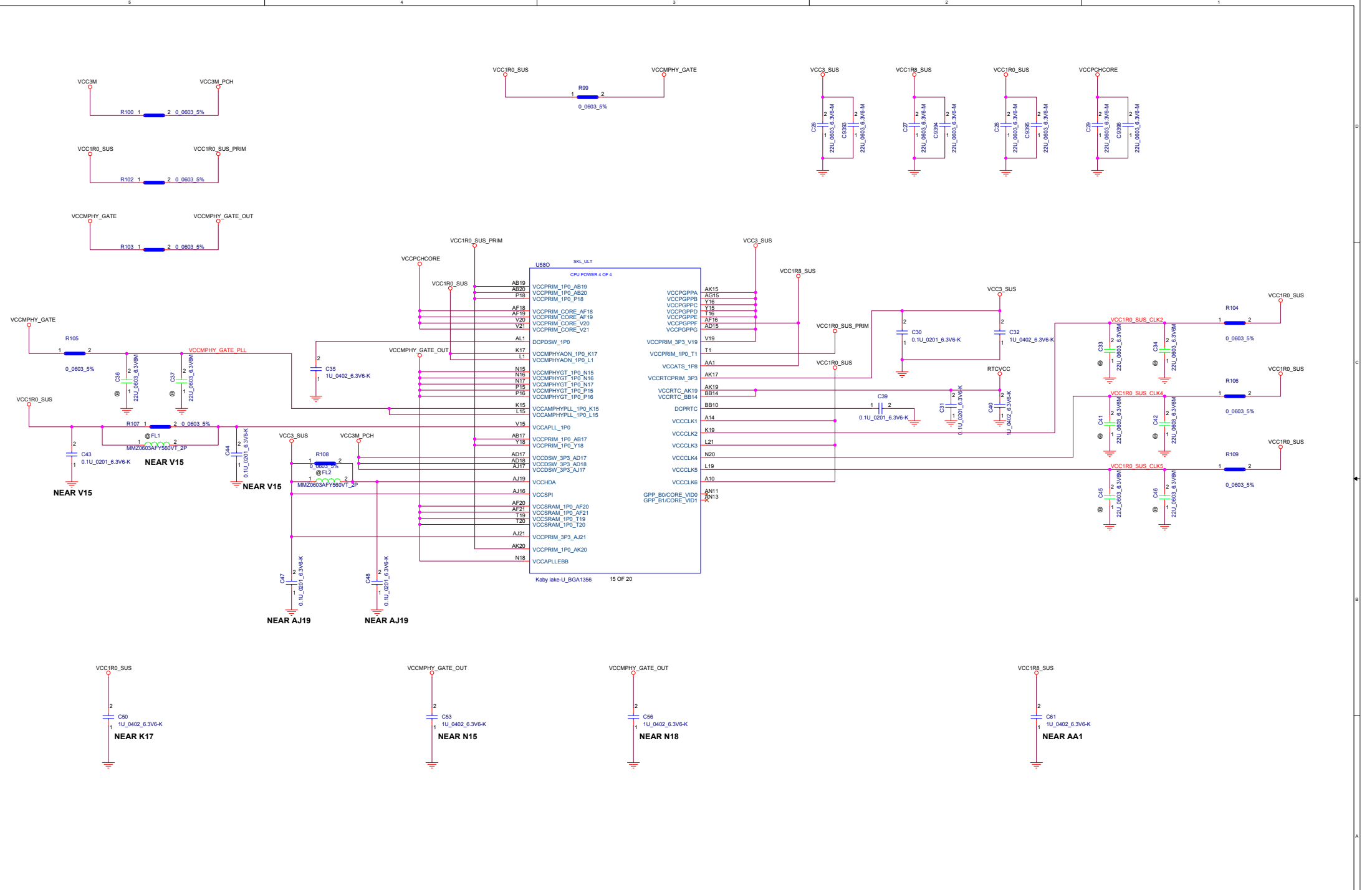
TABLE R90,R91  
KOA:TLRZZATTD  
VISHAY:VSL0805000002EA9



Logic	Ref Des	KBL-R U42	KBL U22
Page 12	Y1	NO_ASM	ASM
	R67	NO_ASM	ASM
	R66	NO_ASM	ASM
	C4	NO_ASM	ASM
	C5	NO_ASM	ASM
	R10445	NO_ASM	ASM
Page 18	Y3	ASM	NO_ASM
	R114	ASM	NO_ASM
	R110	ASM	NO_ASM
	C63	ASM	NO_ASM
	C64	ASM	NO_ASM
	R10466	ASM	NO_ASM
Page 15	R90	ASM	NO_ASM
	R91	NO_ASM	ASM
	R701	NO_ASM	ASM

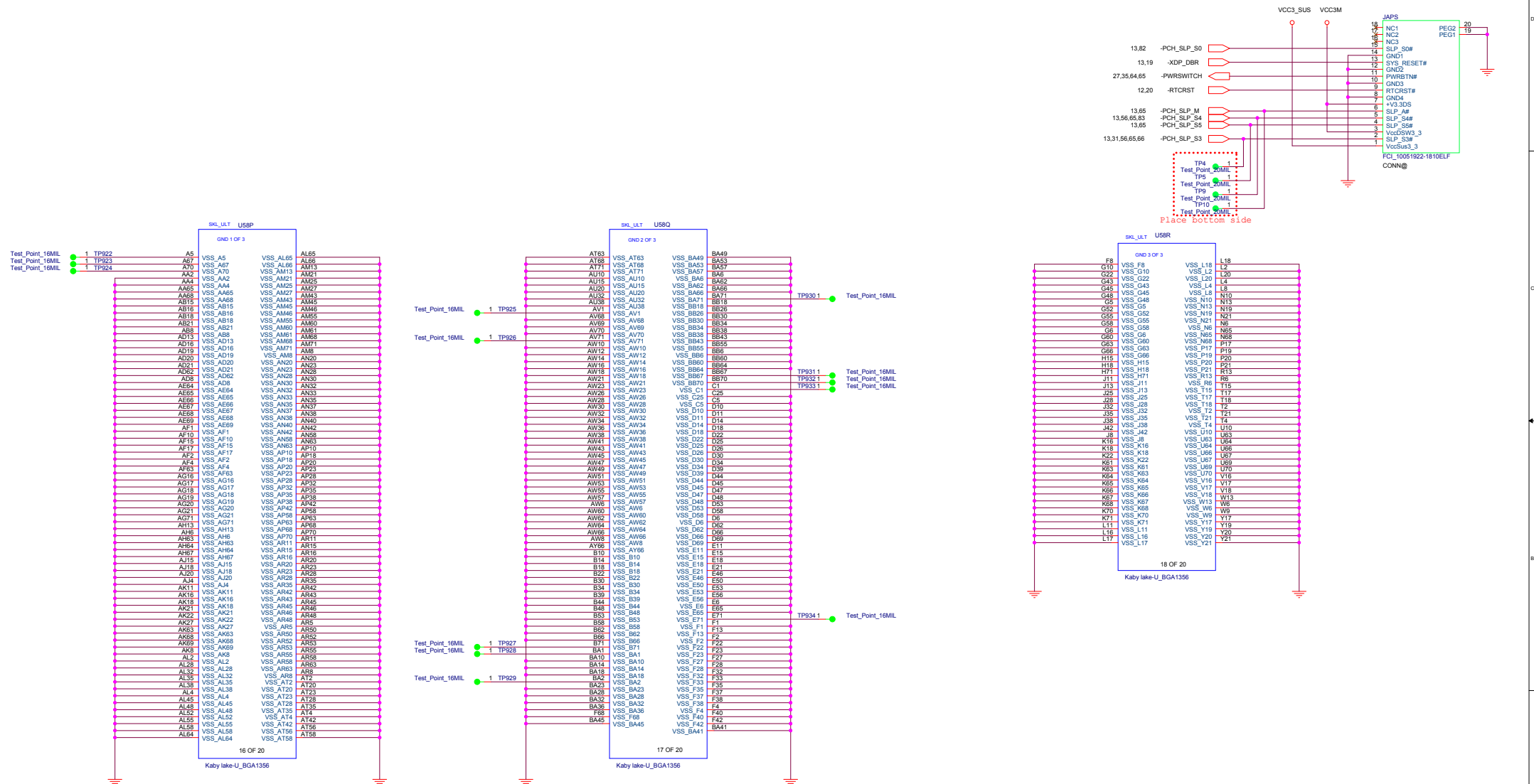
LOGIC







# APS/PETS Interface



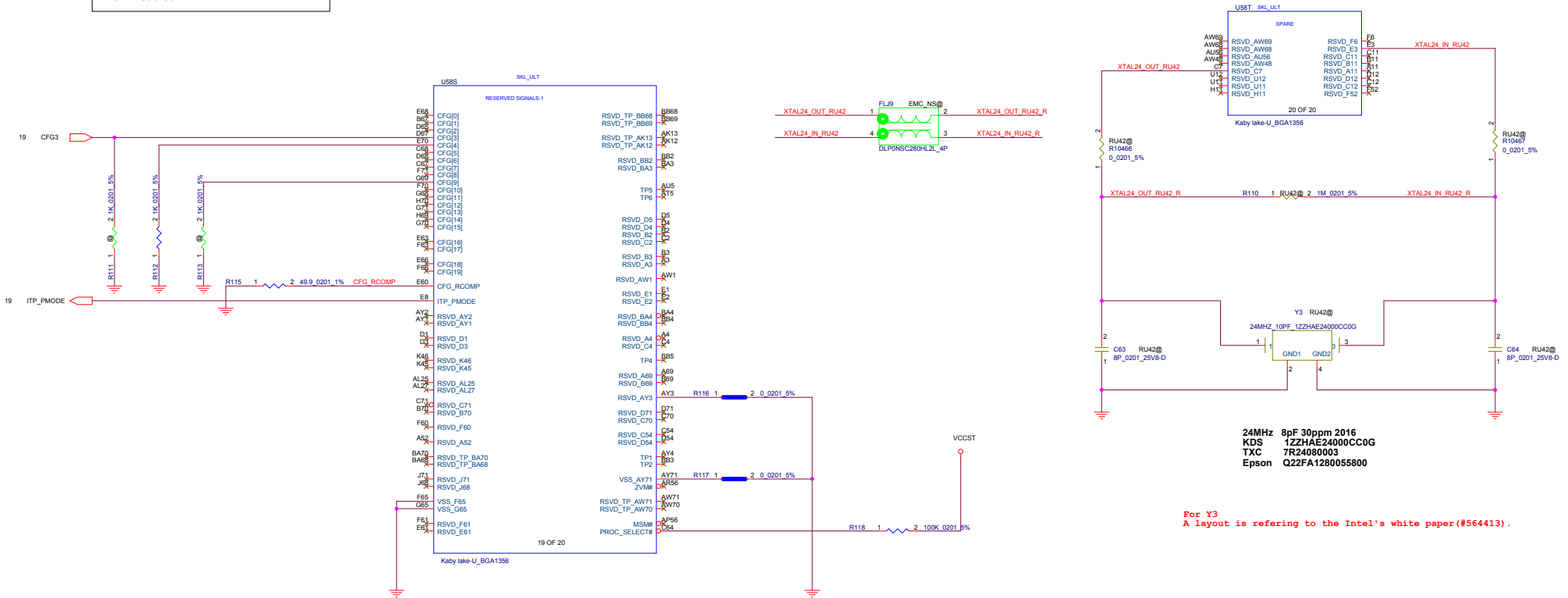
TABLE

**CFG0 : Stall Reset Sequence after PCU PLL Lock until de-asserted**  
 1 : No Stall  
 0 : Stall

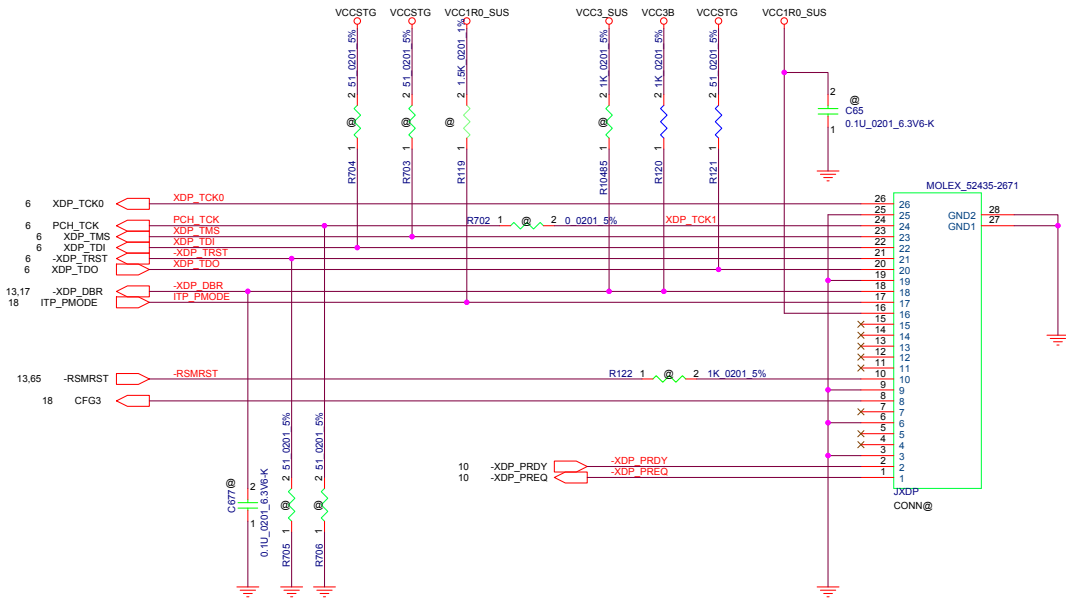
**CFG3 : MSR Privacy Bit Feature**  
 1 : MSR (C80h) bit[0] setting  
 0 : MSR (C80h) bit[0] overridden

**CFG4 : eDP Enable**  
 1 : Disabled  
 0 : Enabled

**CFG9 : SVID Bus Communication**  
 1 : Enabled  
 0 : Disabled



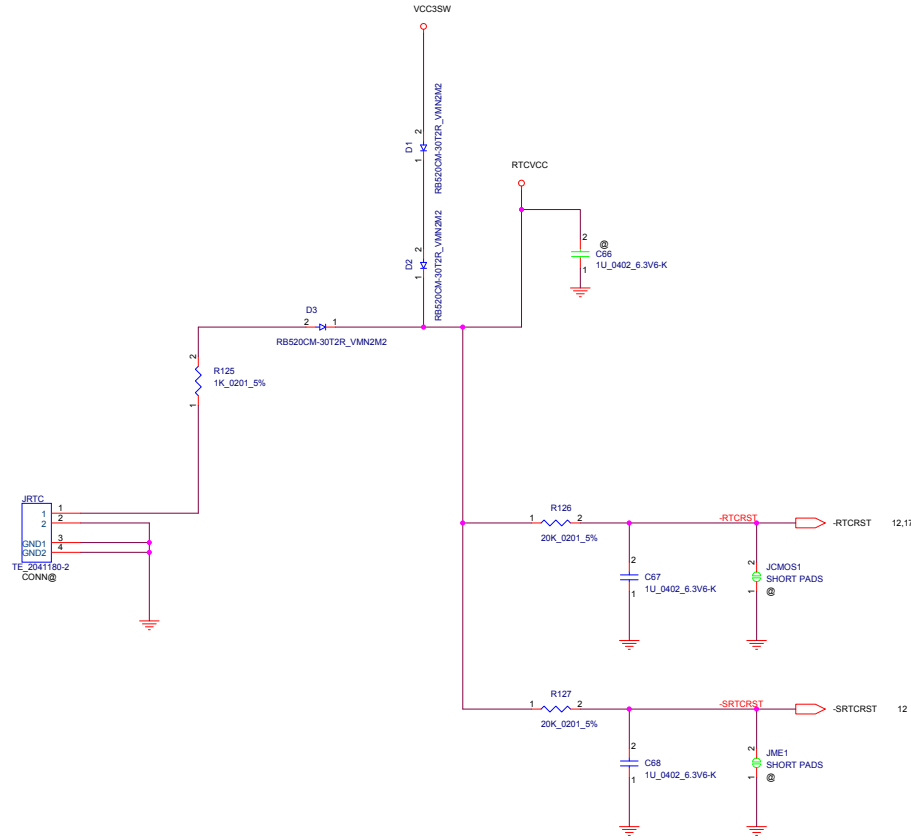
For Y3  
 A layout is referring to the Intel's white paper(#564413).



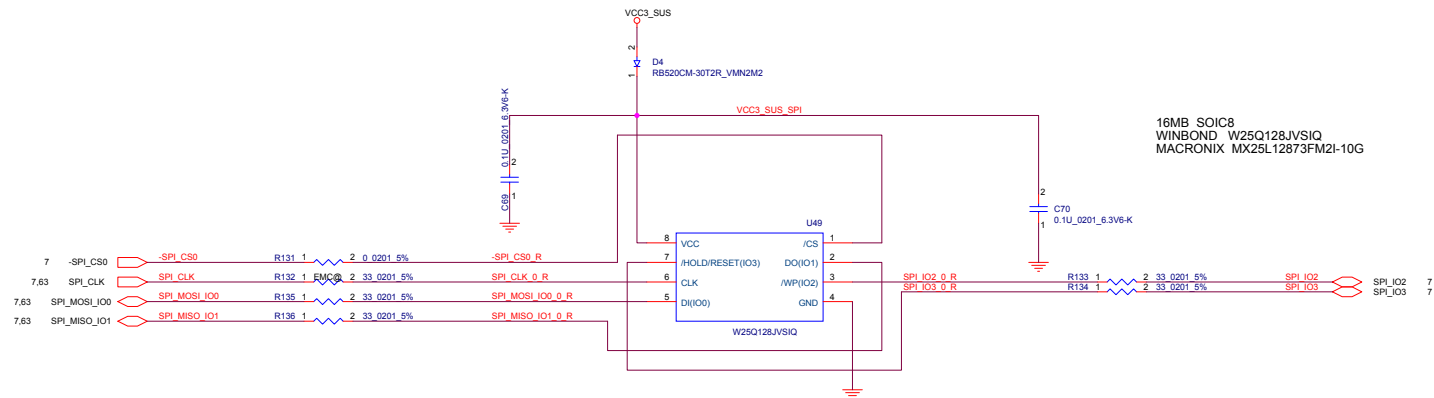
TABLE

Logic	Ref Des	Merged	DCI 2.0
Page 7	R33	ASM	NO_ASM
Page 18	R111	ASM	NO_ASM
Page 19	J8	ASM	NO_ASM
	C65	ASM	NO_ASM
	R121	ASM	ASM
	R120	ASM	ASM
	R119	ASM	NO_ASM
	R122	ASM	NO_ASM
	R702	ASM	NO_ASM

↑  
LOGIC



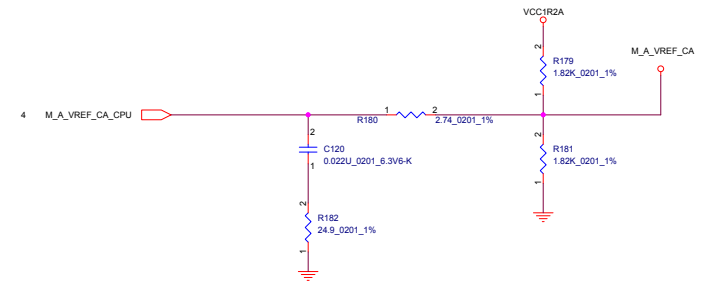
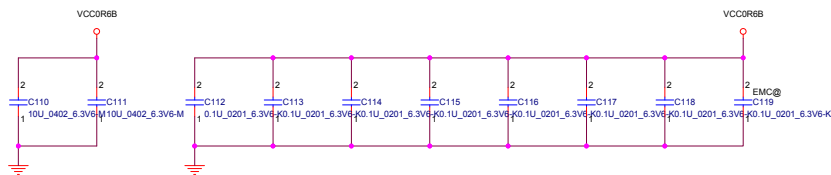
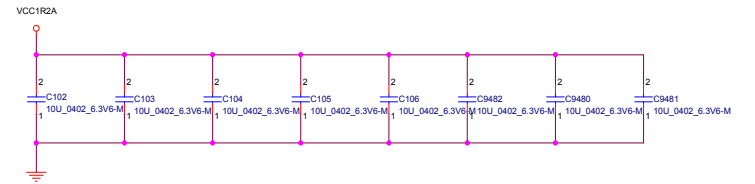
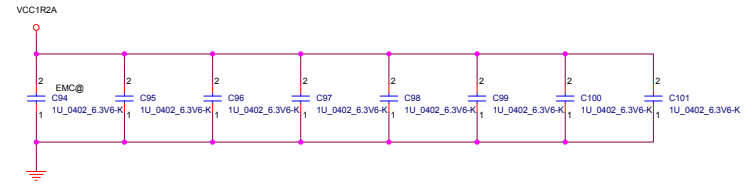
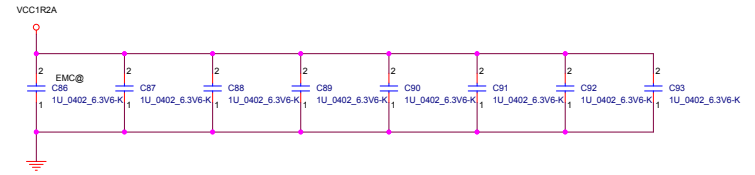
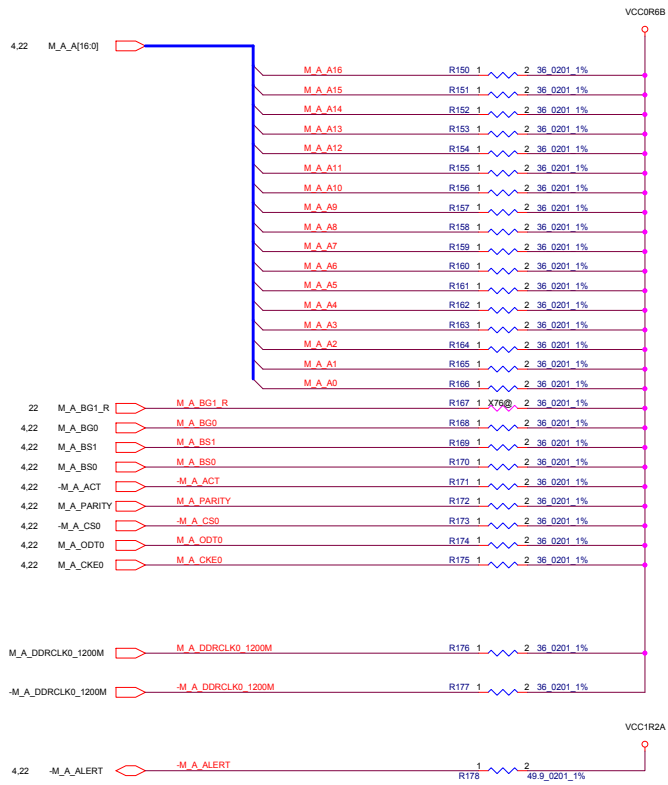
LC Future Center Secret Data		Project Name	
LCFC		Kolar-1	
Rev	Title	RTC BATTERY	
4.02		Date: Wednesday, November 01, 2017/Sheet 20 of 97	



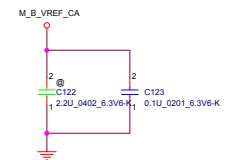
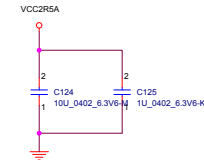
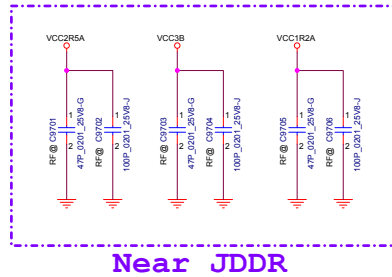
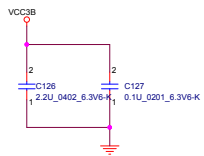
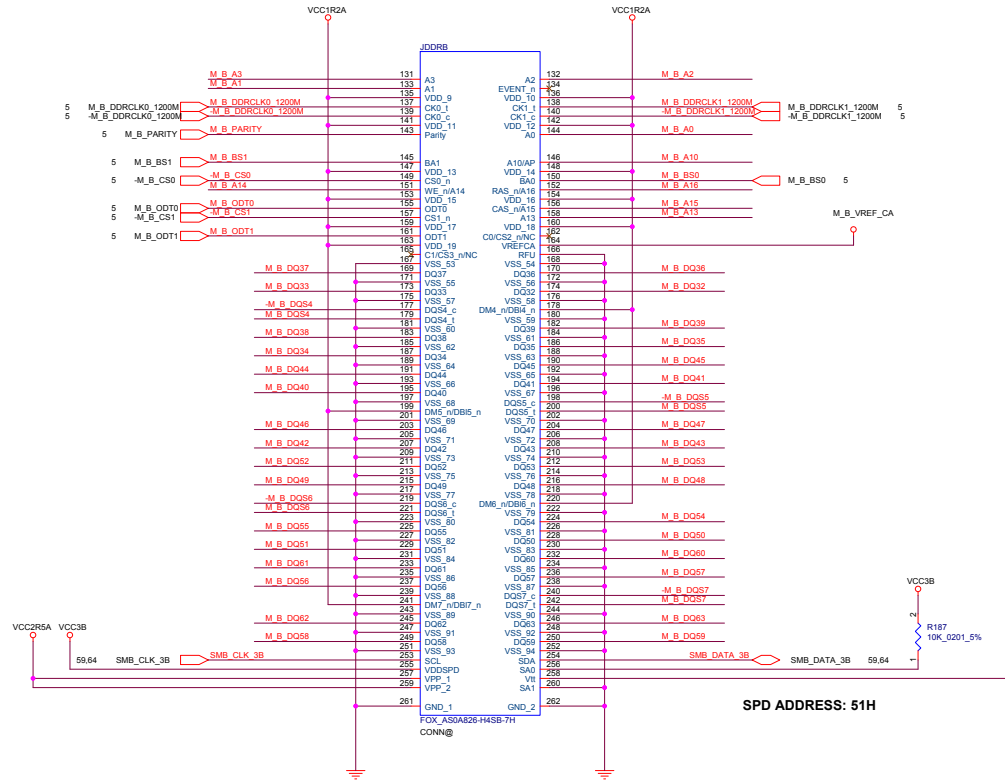
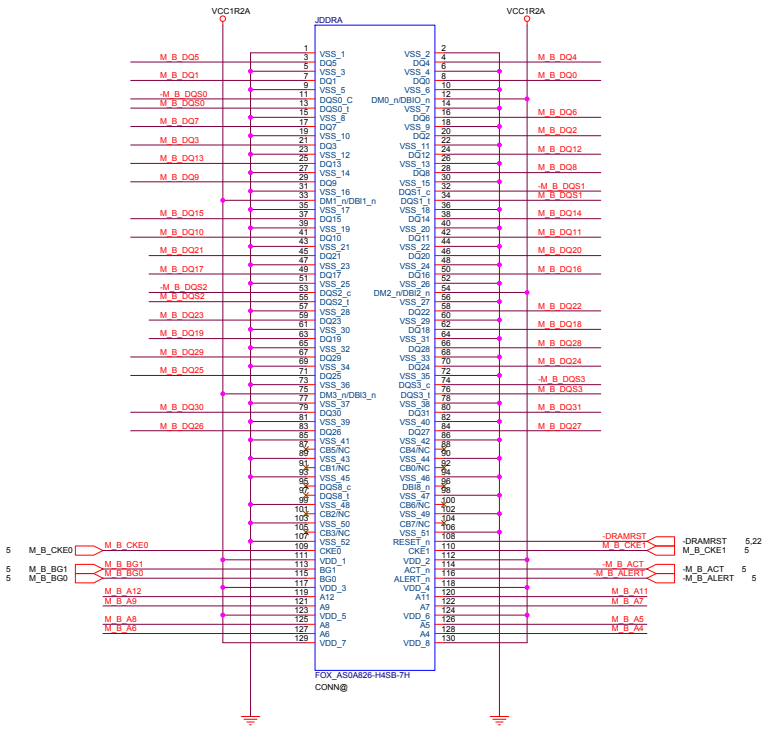
TABLE

SF100 PIN HEADER INTERFACE (TOP VIEW)							
1	VCC	D4.1	GND	GND	2		
3	CS#	R131.2	R132.2	CLK	4		
5	MISO	R136.2	R135.2	MOSI	6		
7	(KEY)	N/A	N/A	(RESET)	8		

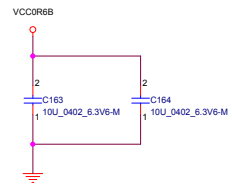
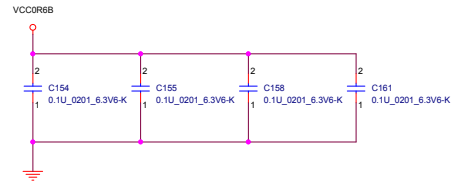
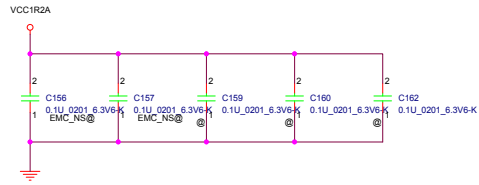
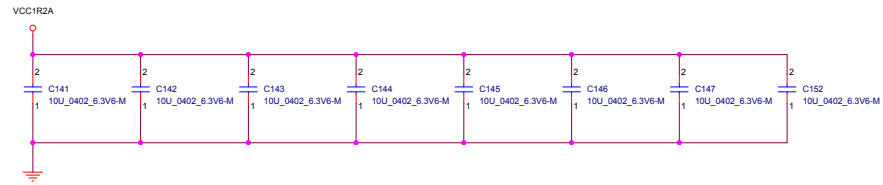
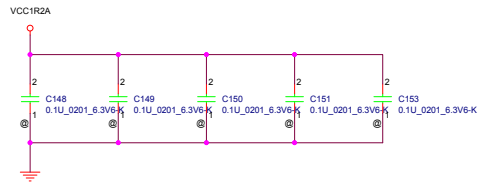
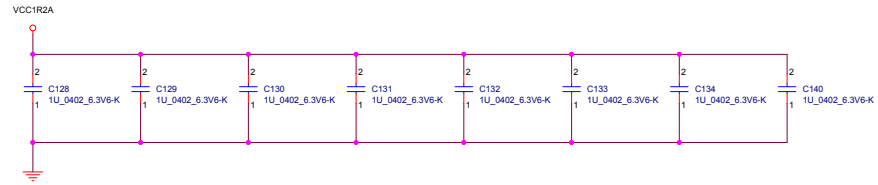
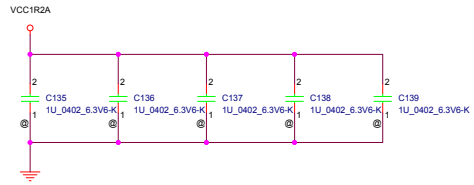


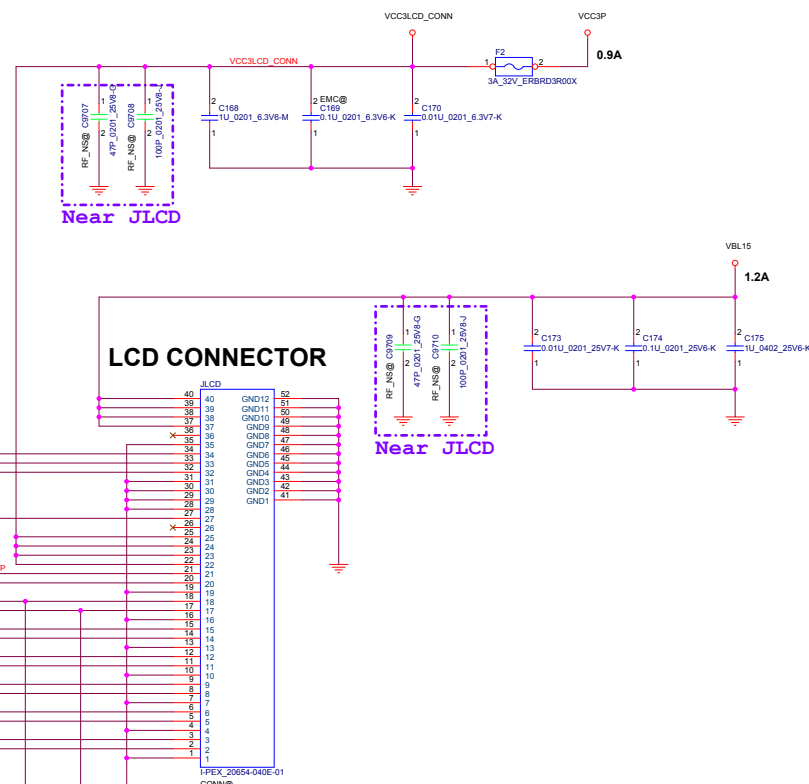
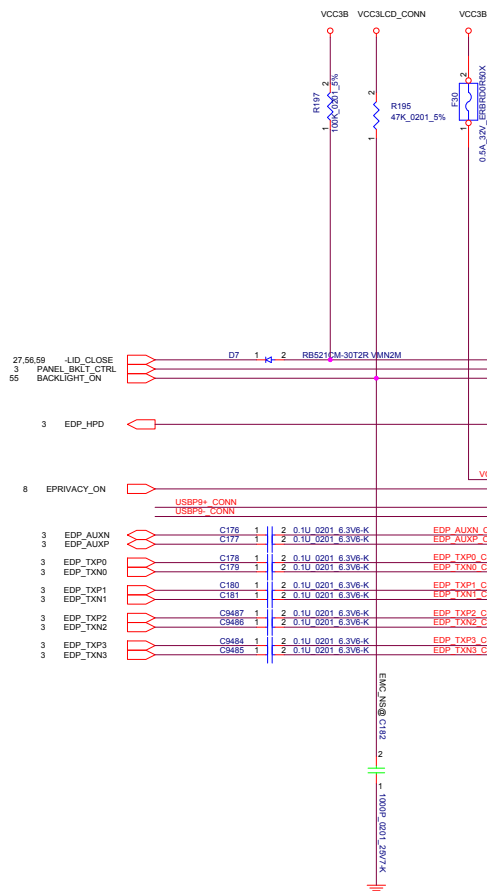
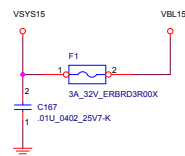


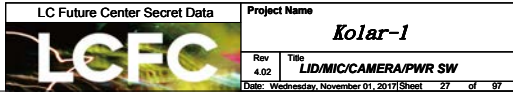
5 M\_B\_DQ[8:0]  
5 -M\_B\_DQS[7:0]  
5 M\_B\_DQS[7:0]  
5 M\_B\_A[16:0]













Pin45 SW	Port Priority Sequence
L	DP Port > TMDS Port
H	TMDS Port > DP Port

VCC3B

R219 1 2 4.7K 0.402 5% PS8337\_PEQ R220 1 2 4.7K 0.402 5%

R221 1 2 4.7K 0.402 5% PS8337\_TMSD\_PRE R222 1 2 4.7K 0.402 5%

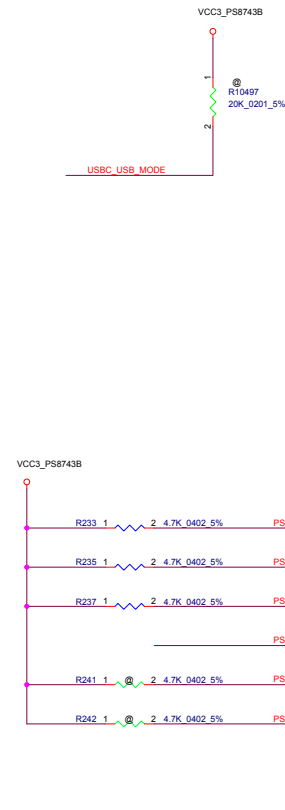
R223 1 2 4.7K 0.402 5% PS8337\_MODE R224 1 2 4.7K 0.402 5%

R225 1 2 4.7K 0.402 5% PS8337\_TMSD\_RT


R227 1 2 4.7K 0.402 5% PS8337\_DP\_CFG0 R228 1 2 4.7K 0.402 5%

R229 1 2 4.7K 0.402 5% PS8337\_TMSD\_DDCBUF R230 1 2 4.7K 0.402 5%

R10492 1 2 4.7K 0.402 5% PS8337\_DP\_CFG1 R10491 1 2 4.7K 0.402 5%



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Date: Wednesday, November 01, 2017 Sheet 30 of 97			



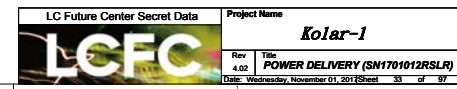


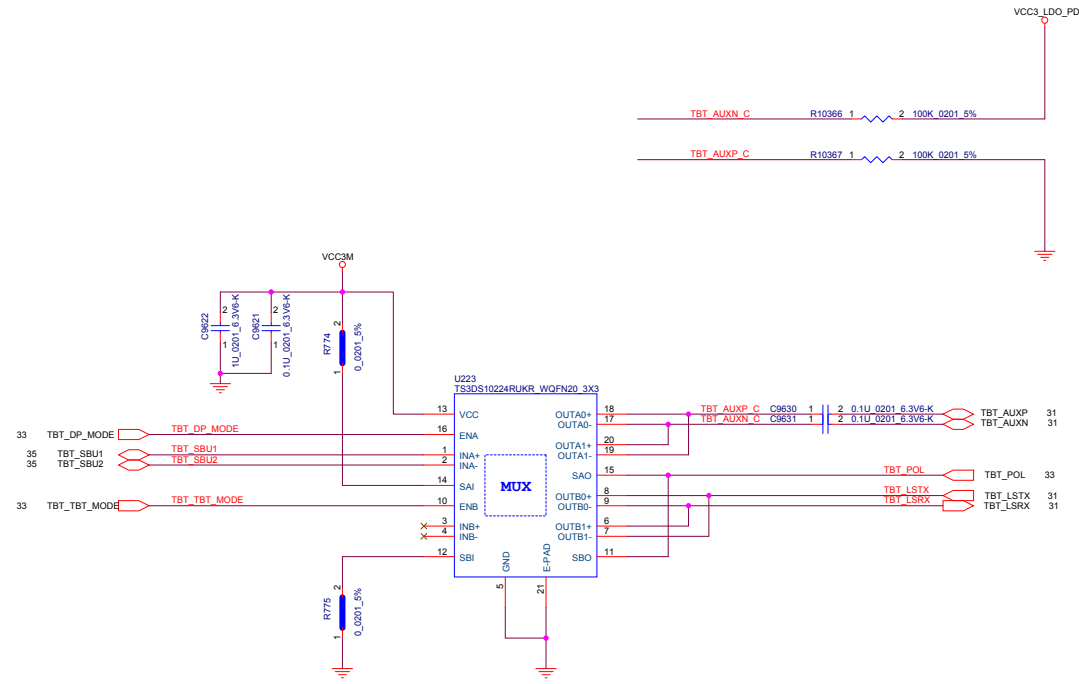


DIV = R301 / (R292 + R301)		CONFIGURATION
DIV MIN	DIV MAX	
0.00	0.18	BP_NoResponse
0.20	0.38	BP_WaitFor3V3_Internal
0.40	0.58	BP_WaitFor3V3_External
0.60	1.00	BP_NoWait

DIV = R302 / (R293 + R302)		I2C Unique Address [3:1]	
DIV MIN	DIV MAX	ADC_ADDR_DECODE_C1	ADC_ADDR_DECODE_C2
0.00	0.18	000b	100b
0.20	0.38	001b	101b
0.40	0.58	010b	110b
0.60	1.00	011b	111b

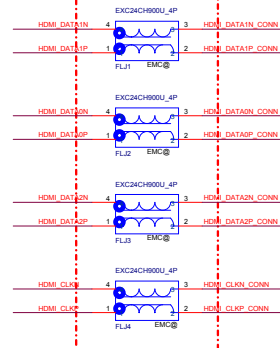
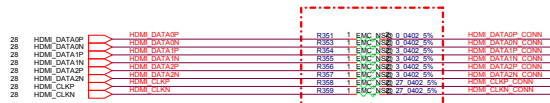
I2C1 (to EC)	TBT PORT	0X23
	USBC PORT	0X27
I2C2 (to AR)	TBT PORT	0X38
	USBC PORT	0X3F



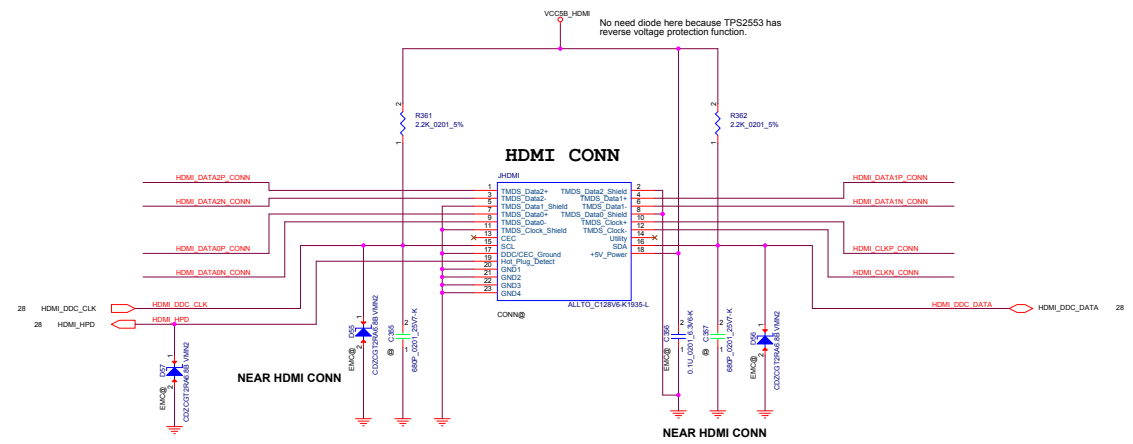
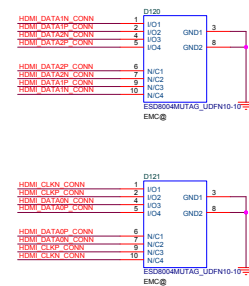
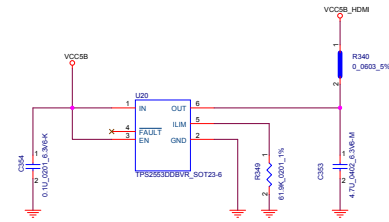






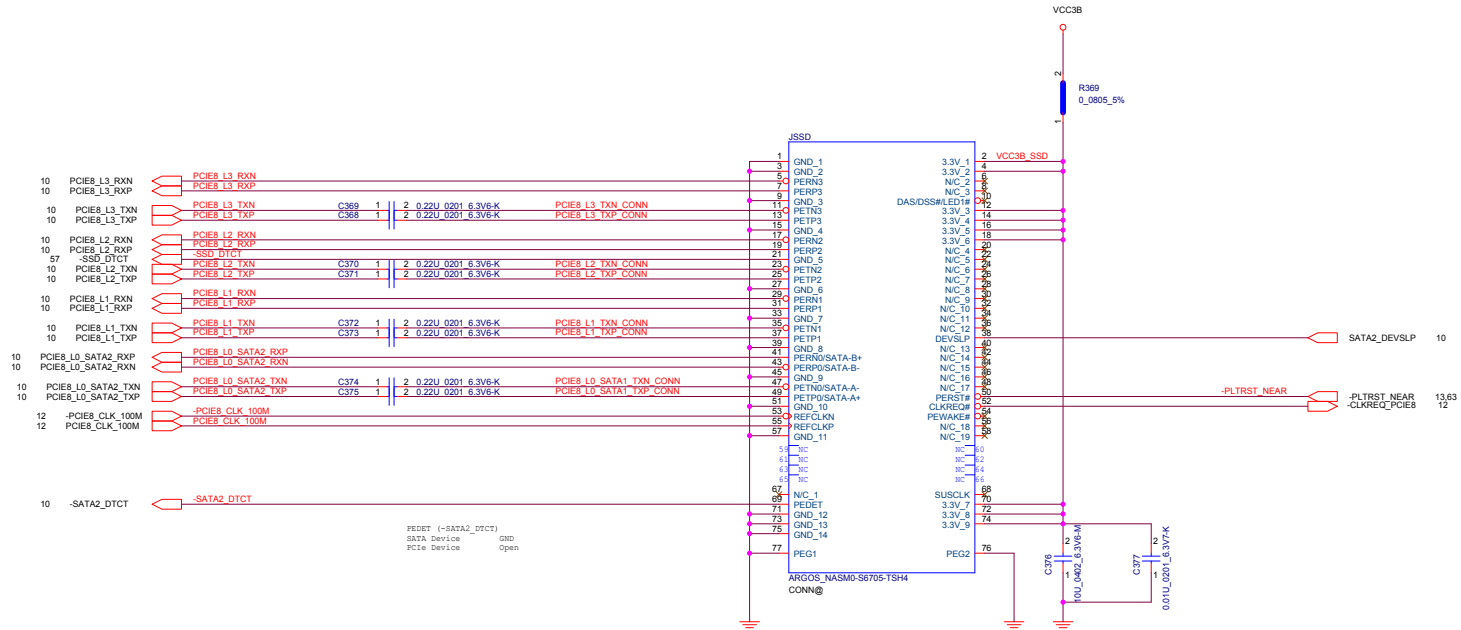


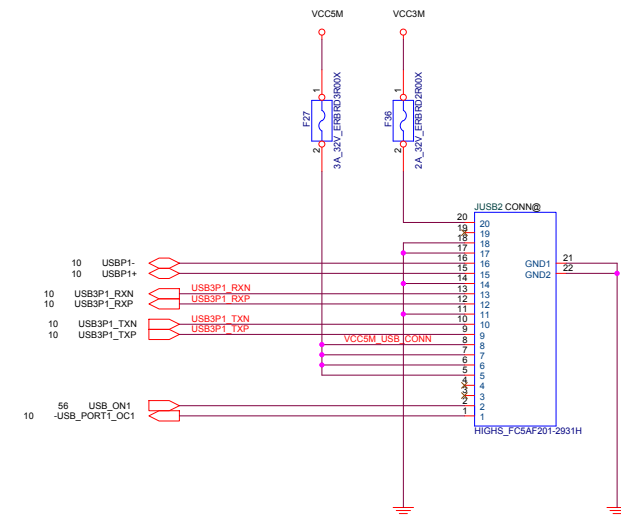
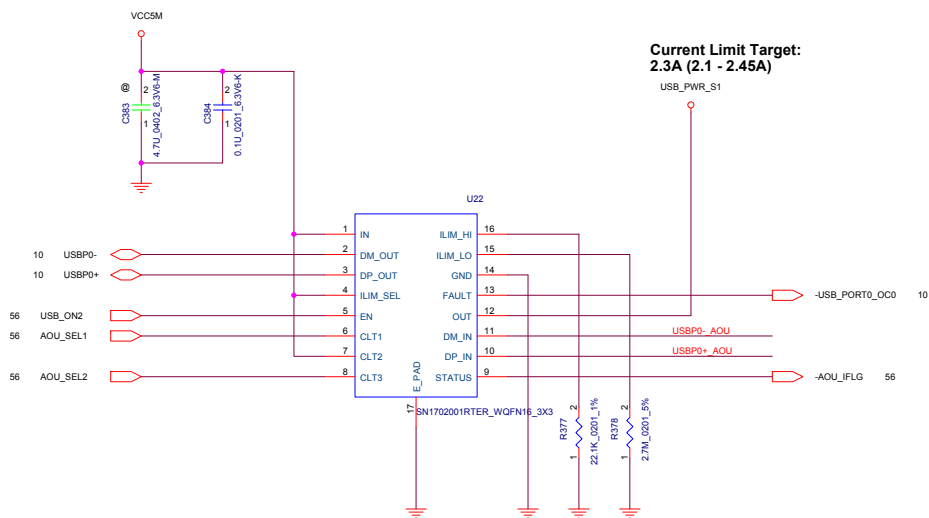
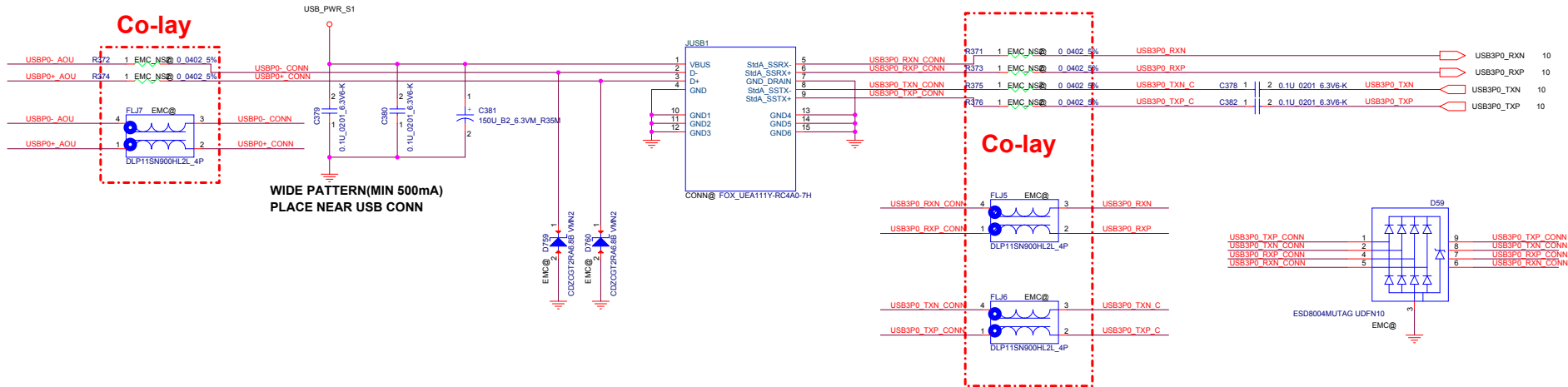
Co-layout




## M.2 Socket 3 (Key-M) for 2280 S3 SSD

H=2.00mm Connector

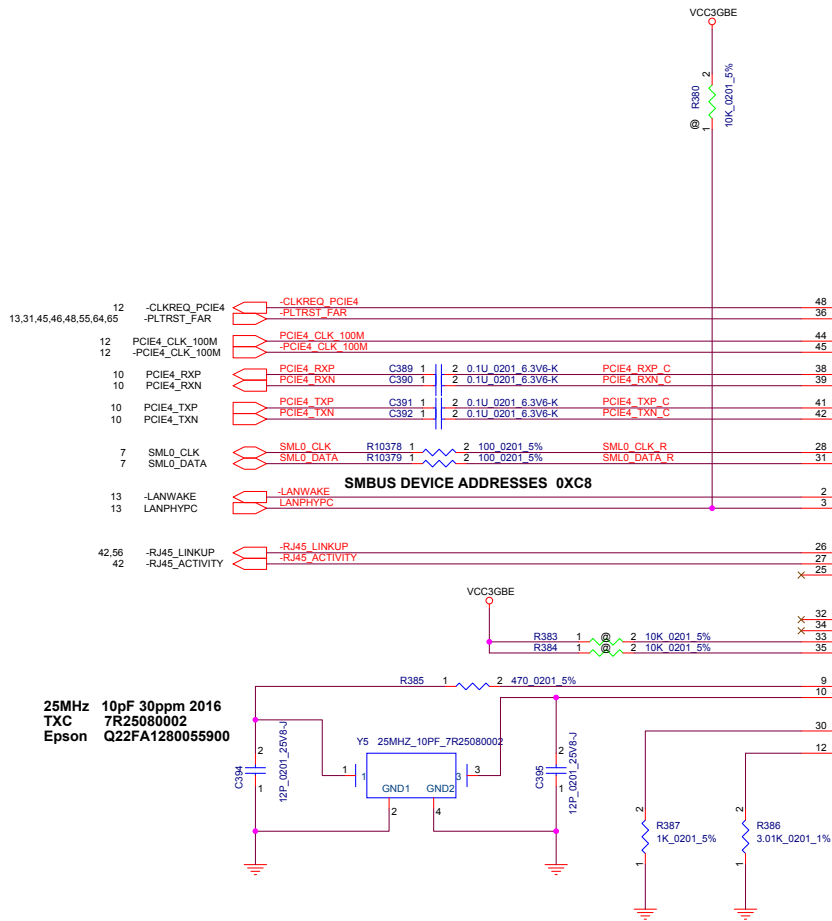




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		4.02	BLANK
Date: Wednesday, November 01, 2017   Sheet 40 of 97			

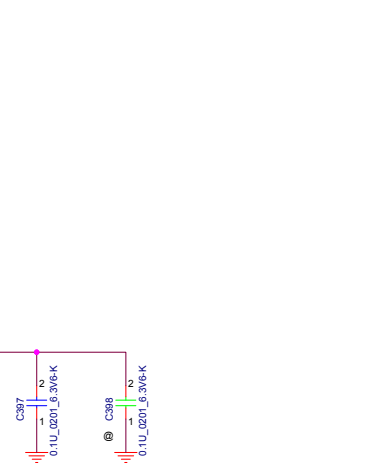
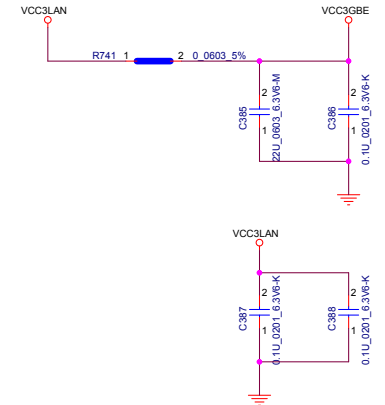
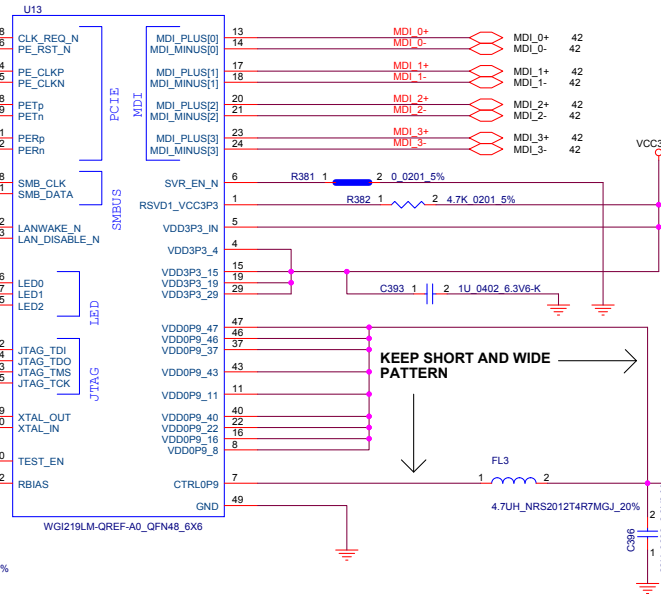




TABLE

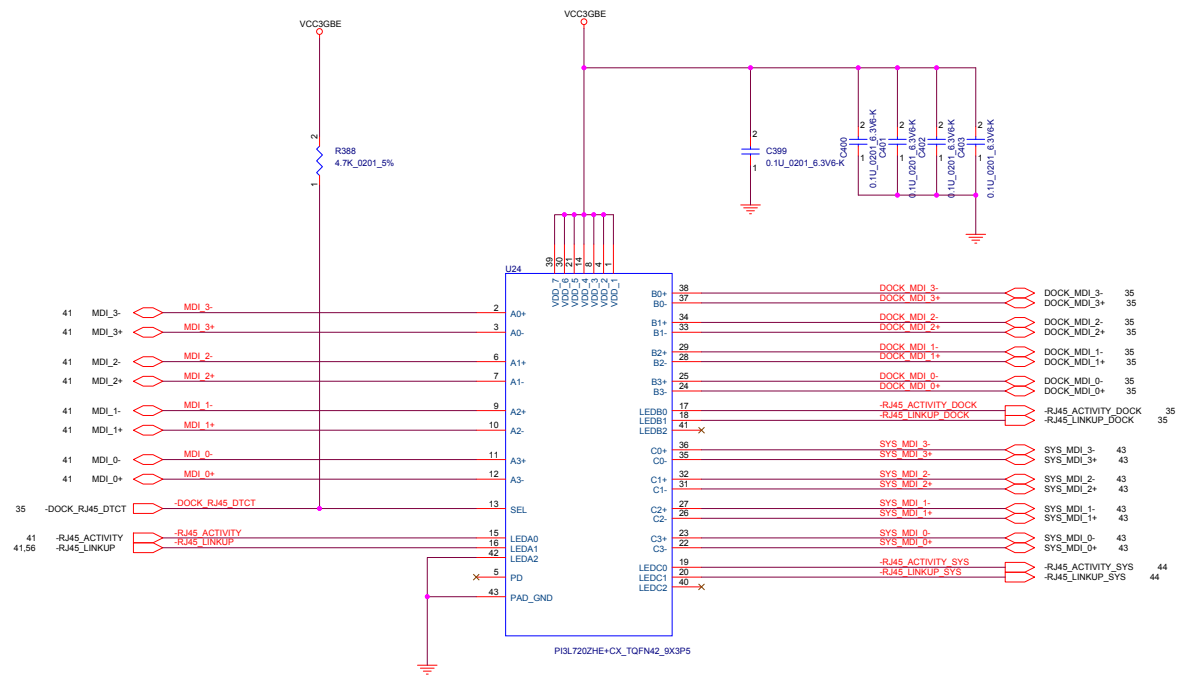
vPro Capability		
GbE PHY	Yes	No
U13	Jacksonville-LM	Jacksonville-V

LOGIC



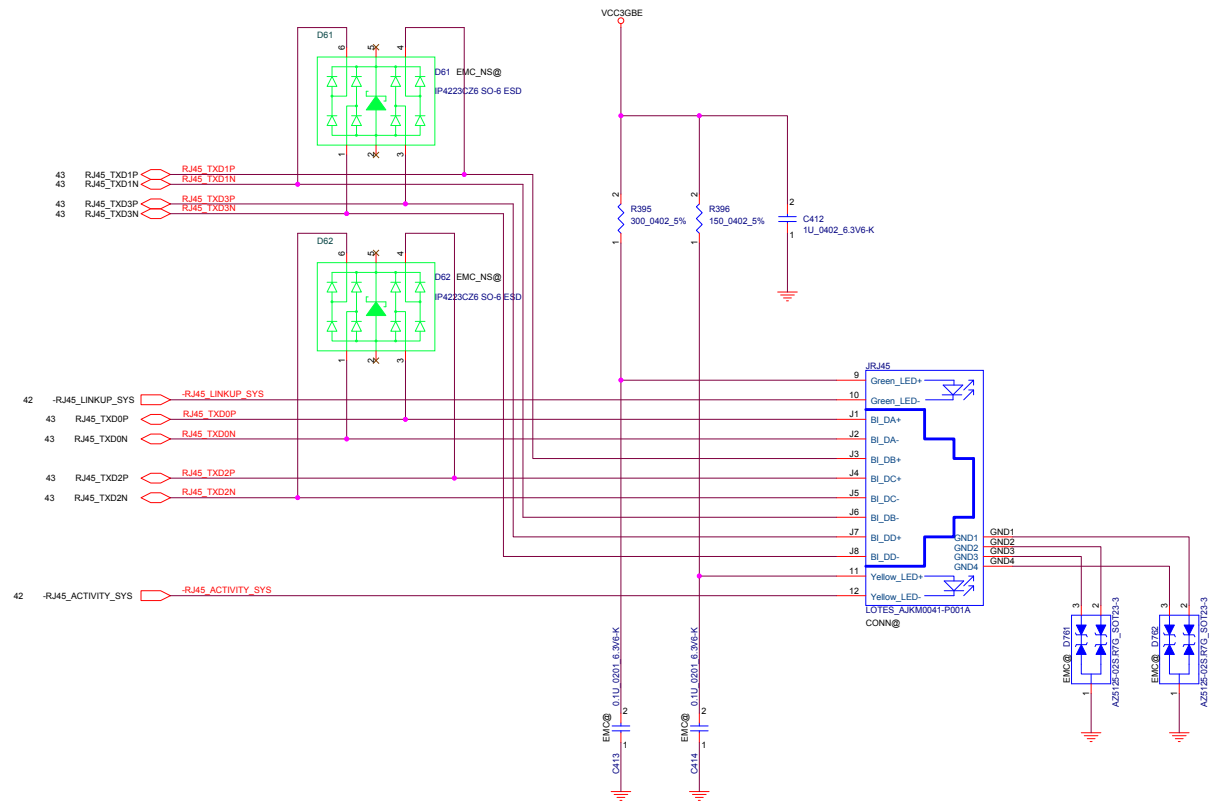
25MHz 10pF 30ppm 2016  
TXC 7R25080002  
Epson Q22FA1280055900

KEEP SHORT AND WIDE PATTERN



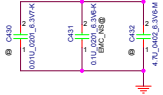
Manufacturer P/N	LCFC P/N
PI3L720ZHE+CX	SA00007E900
TS3L501ERUAR	SA000072400



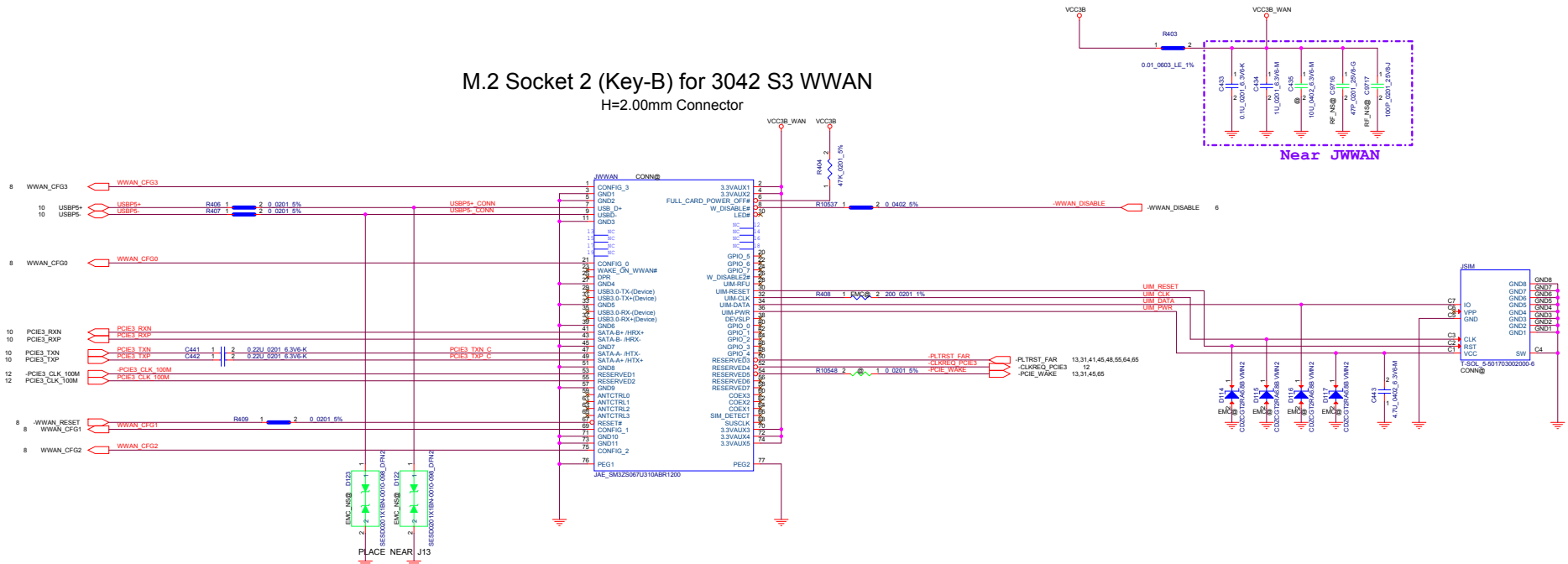


M.2 Socket 1 (Key-A) for 2230 S3 WLAN / Bluetooth / WiGig

H=2.00mm Connector



M.2 Socket 2 (Key-B) for 3042 S3 WWAN  
H=2.00mm Connector



TABLE

	CONFIG 0	CONFIG 3	CONFIG 2	CONFIG 1
Fibocom L830-EB	GND	N.C.	GND	GND
Sierra EM7565	GND	N.C.	N.C.	GND

State#	Module Configuration Decodes				Module Type and Main Host Interface	Port Configuration
	CONFIG_0 (Pin 21)	CONFIG_3 (Pin 1)	CONFIG_2 (Pin 75)	CONFIG_1 (Pin 69)		
0	GND	GND	GND	GND	SSD - SATA	N/A
1	GND	GND	GND	NC	SSD - PCIe	N/A
2	GND	GND	NC	GND	WWAN - PCIe	0
3	GND	GND	NC	NC	WWAN - PCIe	1
4	GND	NC	GND	GND	WWAN - PCIe, USB 3.1 Gen1	0
5	GND	NC	GND	NC	WWAN - PCIe, USB 3.1 Gen1	1
6	GND	NC	NC	GND	WWAN - PCIe, USB 3.1 Gen1	2
7	GND	NC	NC	NC	WWAN - PCIe, USB 3.1 Gen1	3
8	NC	GND	GND	GND	WWAN - SSIC	0
9	NC	GND	GND	NC	WWAN - SSIC	1
10	NC	GND	NC	GND	WWAN - SSIC	2
11	NC	GND	NC	NC	WWAN - SSIC	3
12	NC	NC	GND	GND	WWAN - PCIe	2
13	NC	NC	GND	NC	WWAN - PCIe	3
14	NC	NC	NC	GND	WWAN - PCIe, USB 3.1 Gen1	Vendor Defined
15	NC	NC	NC	NC	no Module Present	N/A

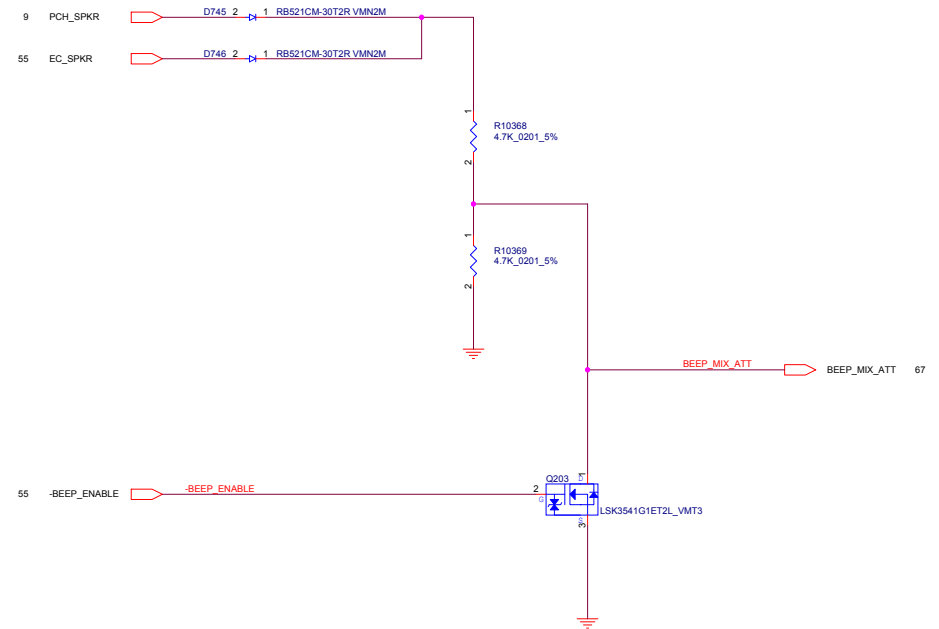
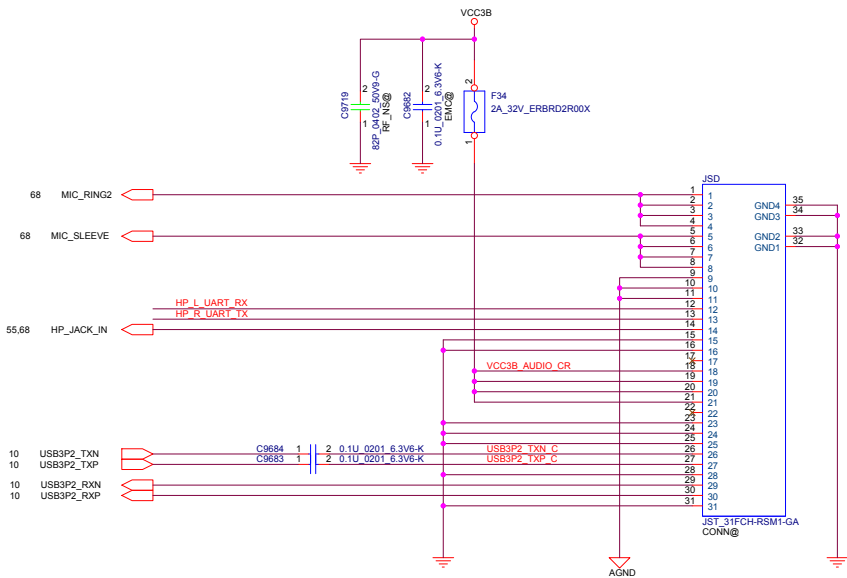


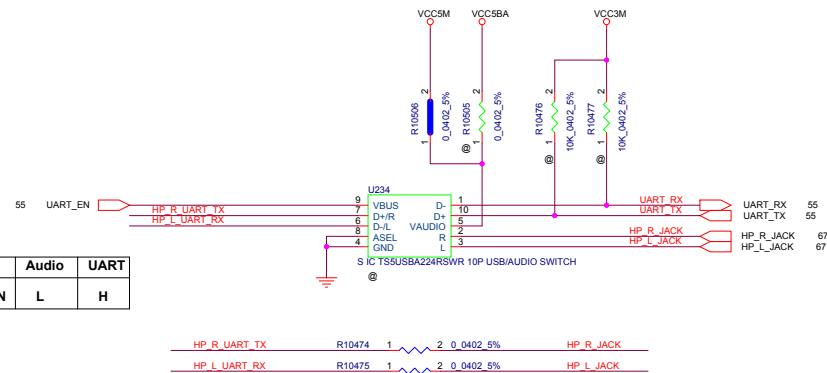
TABLE:

Debug feature	Enable	Disable
U234	ASM	NA
R10476	ASM	NA
R10477	ASM	NA
R10468	Don't care	ASM
R10469	Don't care	ASM
R10470	ASM	NA
R10471	ASM	NA
R10474	NA	ASM
R10475	NA	ASM

↑  
LOGIC

TABLE:

Mode	Audio	UART
UART_EN	L	H











VCCGFXCORE\_D

Place under GPU

C9577  
1U\_0402\_6.3V6-K  
SWG@

C9579  
1U\_0402\_6.3V6-K  
SWG@

C9570  
1U\_0402\_6.3V6-M  
SWG@

C9567  
1U\_0402\_6.3V6-M  
SWG@

C9568  
1U\_0402\_6.3V6-M  
SWG@

C9569  
1U\_0402\_6.3V6-M  
SWG@

Place near GPU

C9571  
1U\_0603\_25V6-M  
SWG@

C9572  
1U\_0603\_25V6-M  
SWG@

C9574  
1U\_0603\_25V6-M  
SWG@

C9576  
1U\_0603\_25V6-M  
SWG@

C9578  
1U\_0603\_25V6-M  
SWG@

C9580  
1U\_0603\_25V6-M  
SWG@

C9581  
1U\_0603\_25V6-M  
SWG@

Place near GPU

C9526  
1U\_0402\_6.3V6-M  
SWG@

C9523  
1U\_0402\_6.3V6-M  
SWG@

C9525  
1U\_0402\_6.3V6-M  
SWG@

C9524  
1U\_0402\_6.3V6-M  
SWG@

U47F

7/14 VDD5

L11  
VDD5\_1  
L17  
VDD5\_2  
M14  
VDD5\_3  
P10  
VDD5\_4  
P12  
VDD5\_5  
P16  
VDD5\_6  
P18  
VDD5\_7  
Y14  
VDD5\_8  
U11  
VDD5\_9  
U17  
VDD5\_10

GM108

RSVD

RSVD

N17S-LG-A1\_GB2C64-595

SWG@

VDD5\_SENSE

GNDS\_SENSE

VCCGFXCORE\_D

U47G

6/14 XVDD

G1  
XVDD\_1  
G2  
XVDD\_2  
G3  
XVDD\_3  
G4  
XVDD\_4  
G5  
XVDD\_5  
G6  
XVDD\_6  
H3  
XVDD\_7  
H4  
XVDD\_8  
H5  
XVDD\_9  
J1  
XVDD\_10  
J2  
XVDD\_11  
J3  
XVDD\_12  
J4  
XVDD\_13  
J5  
XVDD\_14  
J6  
XVDD\_15  
J7  
XVDD\_16  
K1  
XVDD\_17  
K2  
XVDD\_18  
K3  
XVDD\_19  
K4  
XVDD\_20  
K5  
XVDD\_21  
K6  
XVDD\_22  
K7  
XVDD\_23  
L3  
XVDD\_24  
L4  
XVDD\_25  
M1  
XVDD\_26  
M2  
XVDD\_27  
M3  
XVDD\_28  
M4  
XVDD\_29  
M5  
XVDD\_30  
M6  
XVDD\_31  
N1  
XVDD\_32  
N2  
XVDD\_33  
N3  
XVDD\_34  
XVDD\_35

XVDD\_36

XVDD\_37

XVDD\_38

XVDD\_39

XVDD\_40

XVDD\_41

XVDD\_42

XVDD\_43

XVDD\_44

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XVDD\_110

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XVDD\_292

XVDD\_293

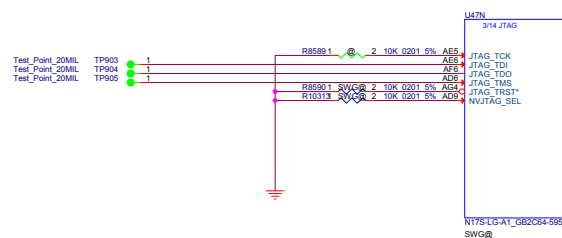
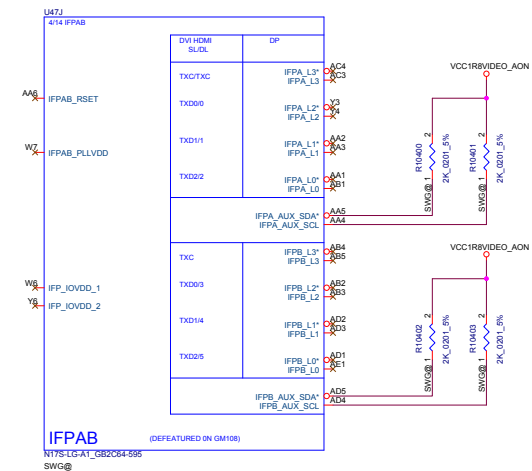
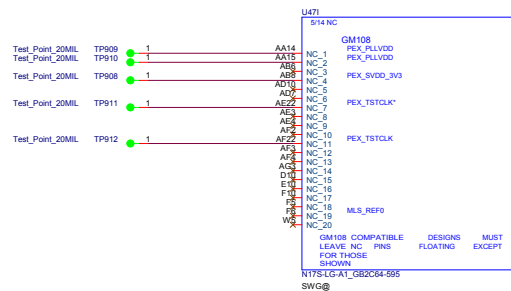
XVDD\_294

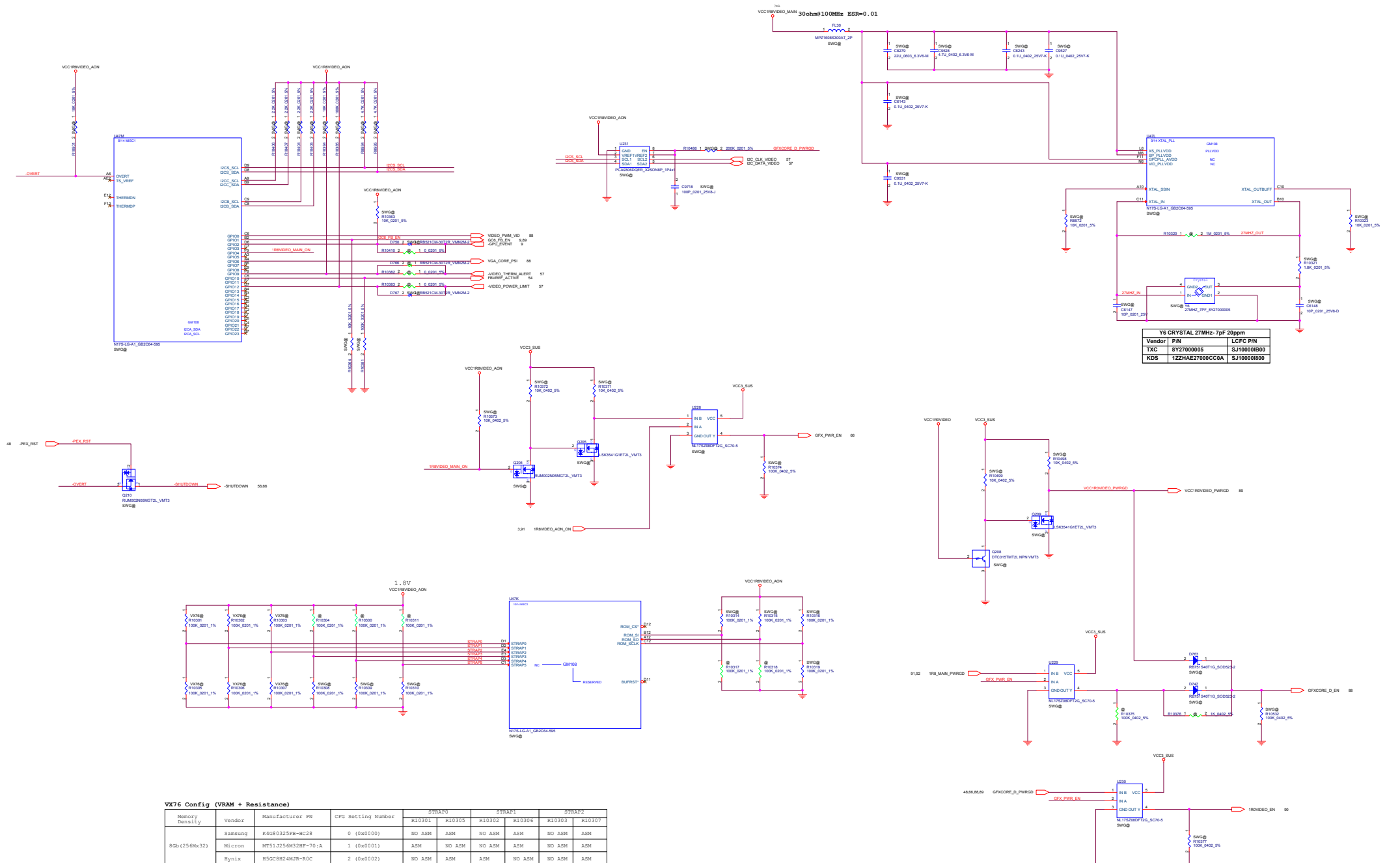
XVDD\_295

XVDD\_296

XVDD\_297

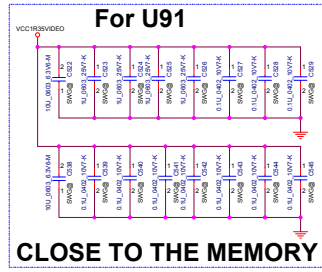
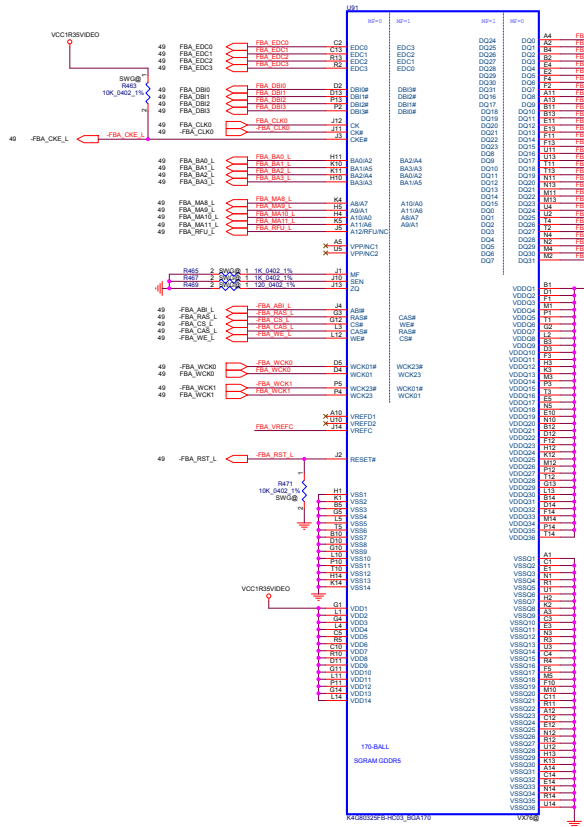
XVDD\_298



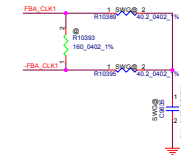
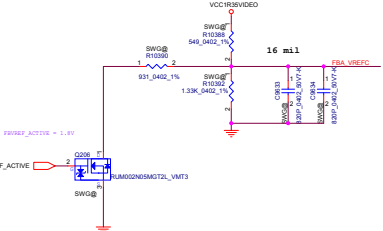
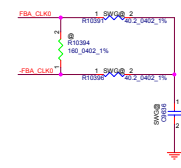
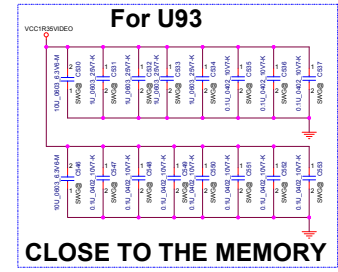
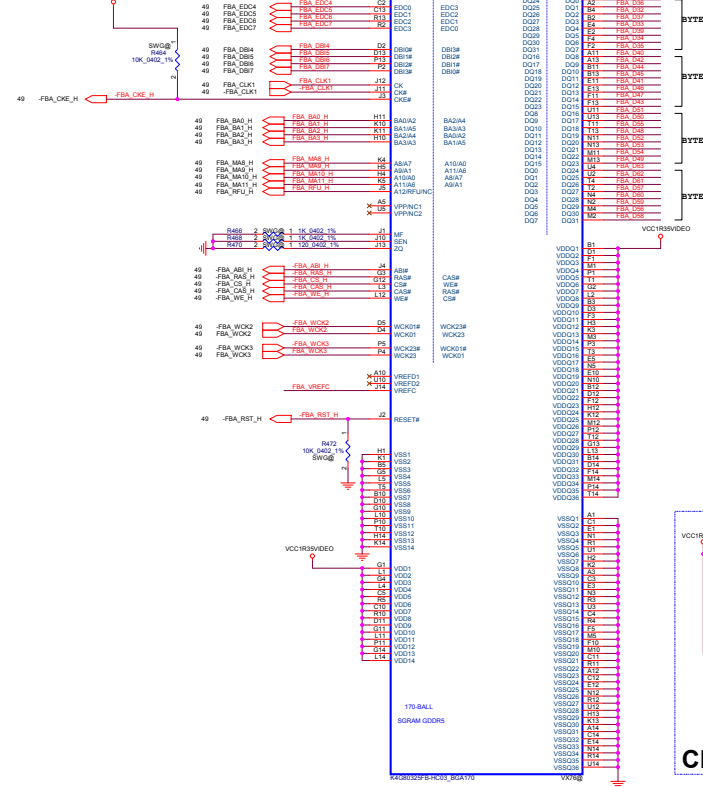


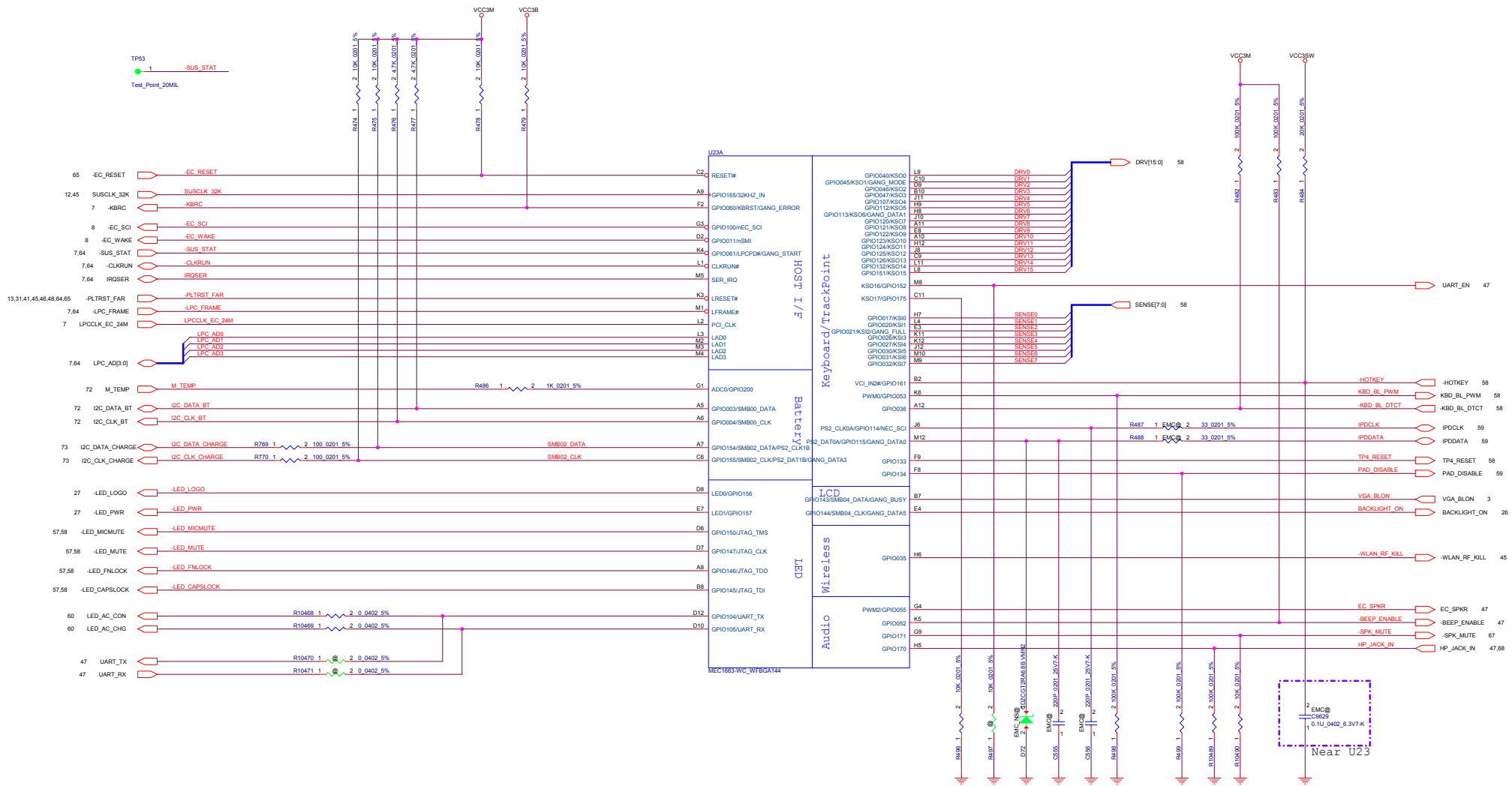
40 FBA\_CLK\_0

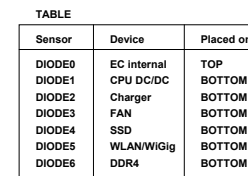
MF=0



40 FBA\_CLK\_1

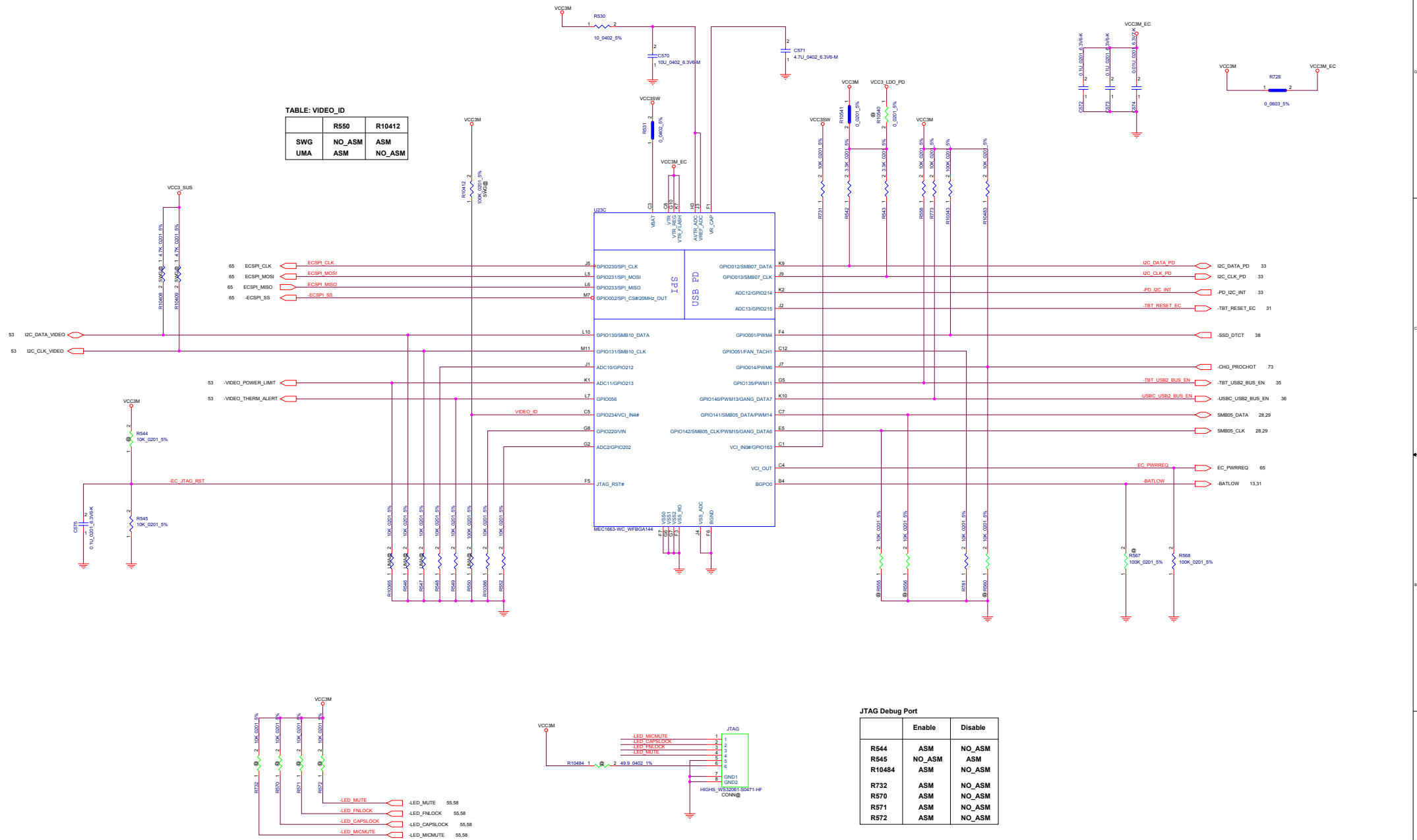




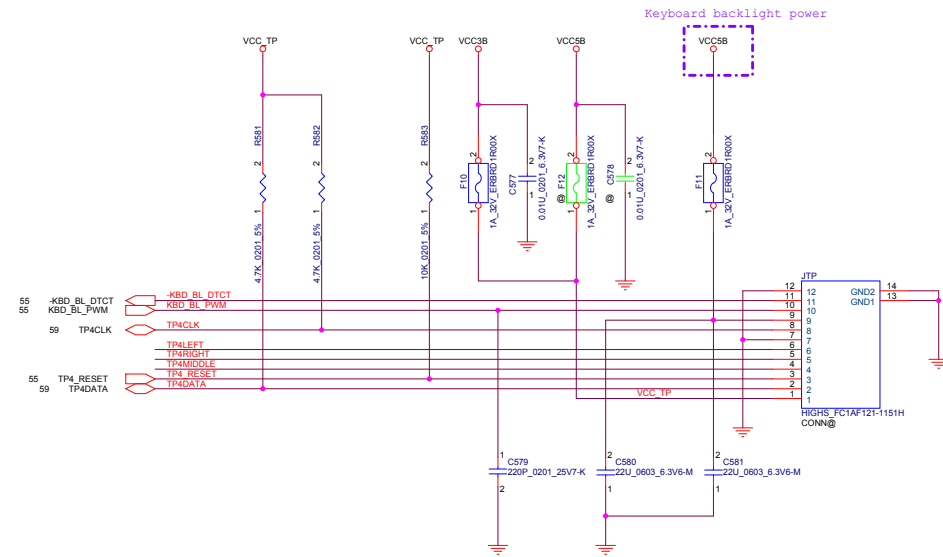
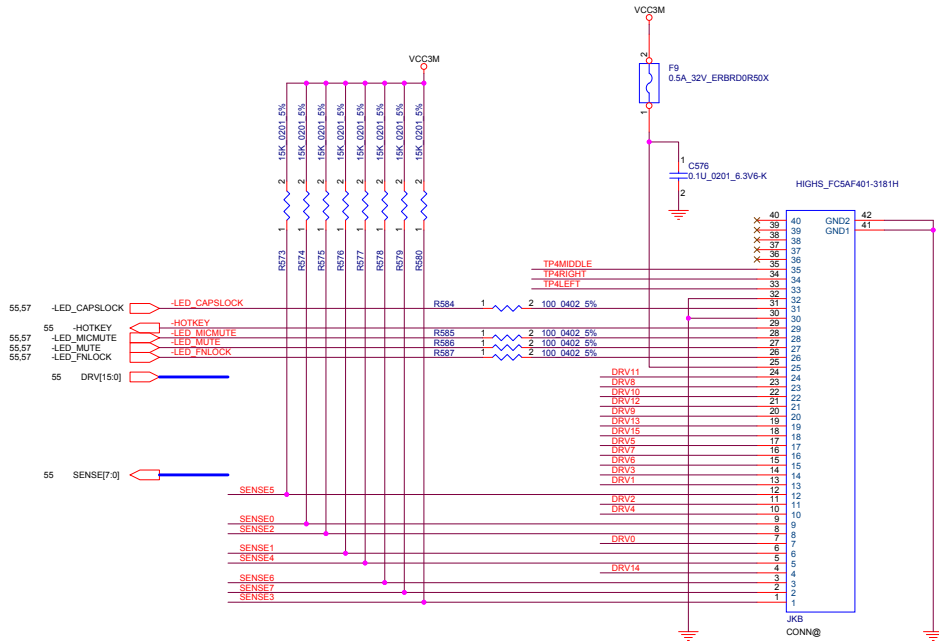


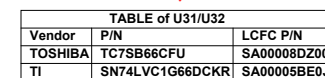
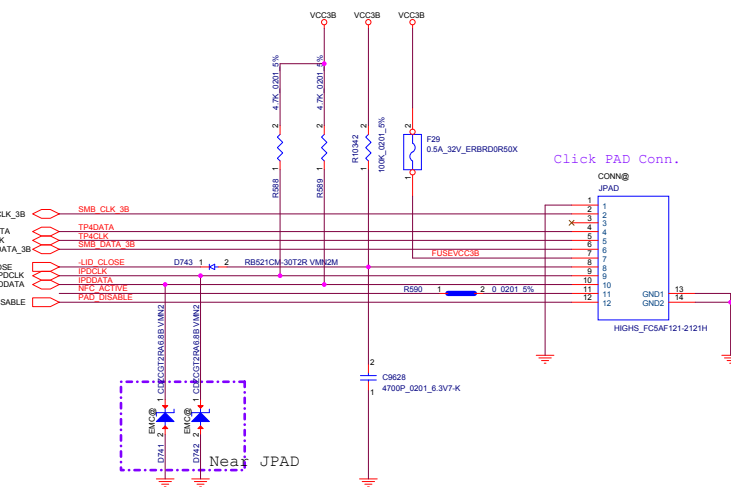


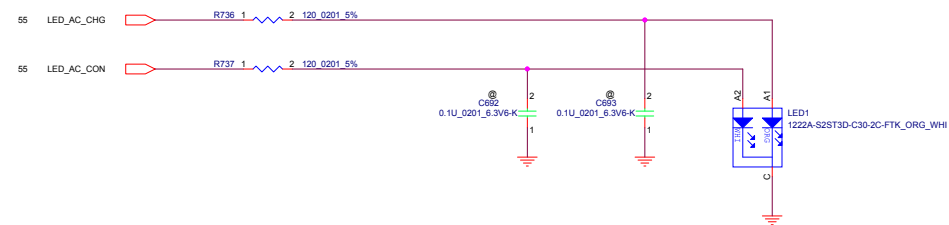
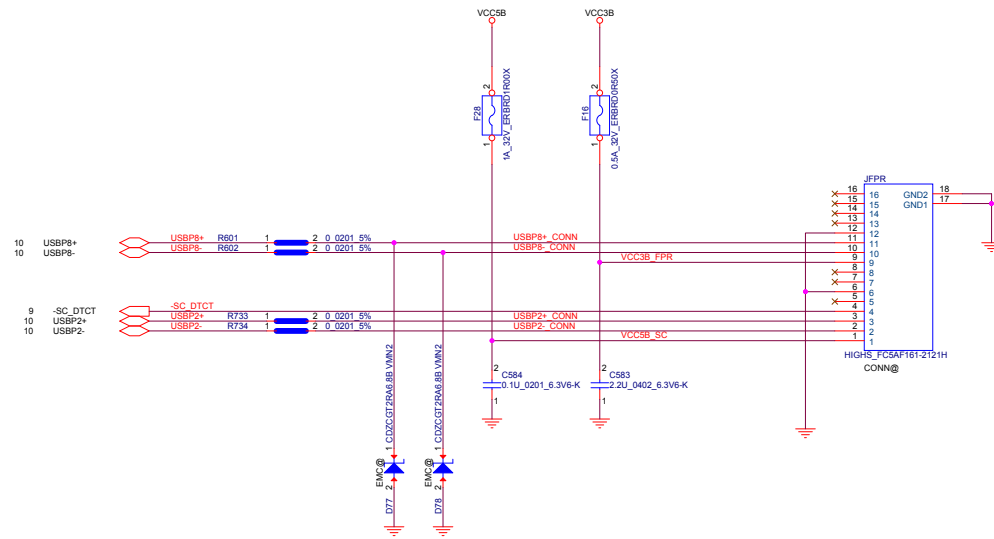
	R550	R10412
SWG	NO_ASM	ASM
UMA	ASM	NO_ASM

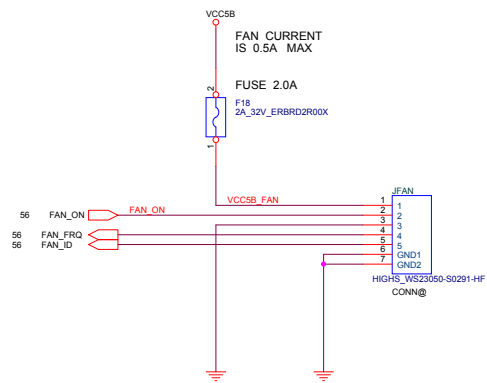


JTAG Debug Port		
	Enable	Disable
R544	ASM	NO_ASM
R545	NO_ASM	ASM
R10484	ASM	NO_ASM
R732	ASM	NO_ASM
R570	ASM	NO_ASM
R571	ASM	NO_ASM
R572	ASM	NO_ASM



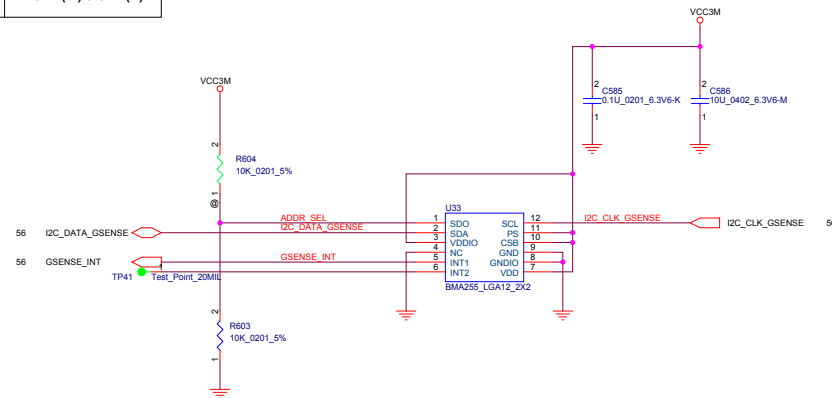






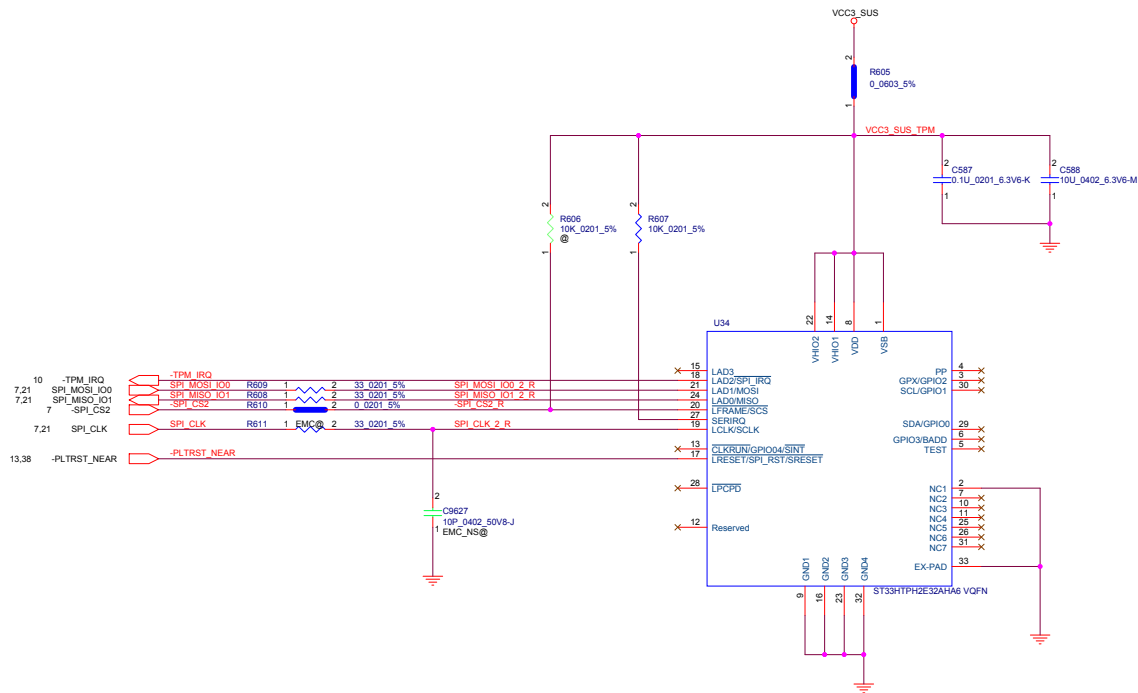
TABLE

P/N	ADDR_SEL	Address
BMA255	H L	32h (W) & 33h (R) 30h (W) & 31h (R)
KX022-1020	H L	3Eh (W) & 3Fh (R) 3Ch (W) & 3Dh (R)



### TABLE of G-Sensor (U148)

Vendor	P/N	LCFC P/N
BOSCH	BMA255	SA00005YJ00
Kionix	KX022-1020	SA000081E00



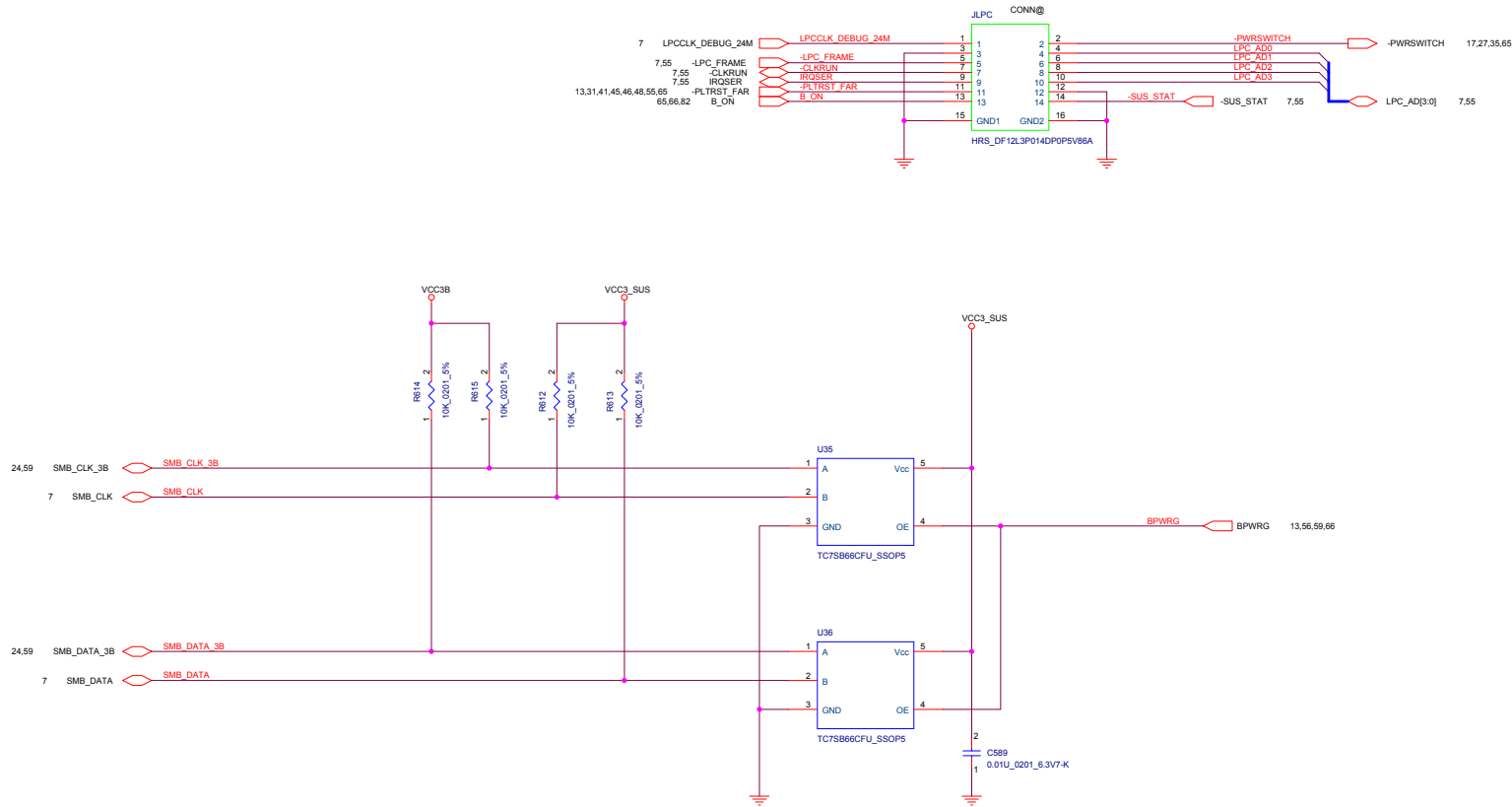
TABLE

Pin No	TCG PTP Spec (v38)	Infineon SLB9670VQ2.0 FW 7.63	ST Micro ST33HTPH2E32AHB4
1	VDD	VDD	NC
2	GND	GND	GND
3	GPIO	NC	NC
4	GPIO	NC	PP
5	NC	NC	NC
6	VNC/GPIO	GPIO	NC
7	GPIO/VDD	PP	GPIO
8	VDD	VDD	NC
9	GND	GND	NC
10	VNC	NC	NC
11	NC	NC	NC
12	NC	NC	NC
13	VNC/GPIO	NC	NC
14	VDD	NC	NC
15	NC	NC	NC
16	GND	NC	NC
17	SPI_RST#	RST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#	SPI_PIRQ#
19	SPI_CLK	SCLK	SPI_CLK
20	SPI_CS#	CS#	SPI_CS#
21	MOSI	MOSI	MOSI
22	VDD	VDD	VPS
23	GND	GND	NC
24	MISO	MISO	MISO
25	NC	NC	NC
26	NC	NC	NC
27	NC	NC	NC
28	NC	NC	NC
29	VNC/GPIO	NC	NC
30	VNC/GPIO	NC	NC
31	VNC	NC	NC
32	GND	GND	NC

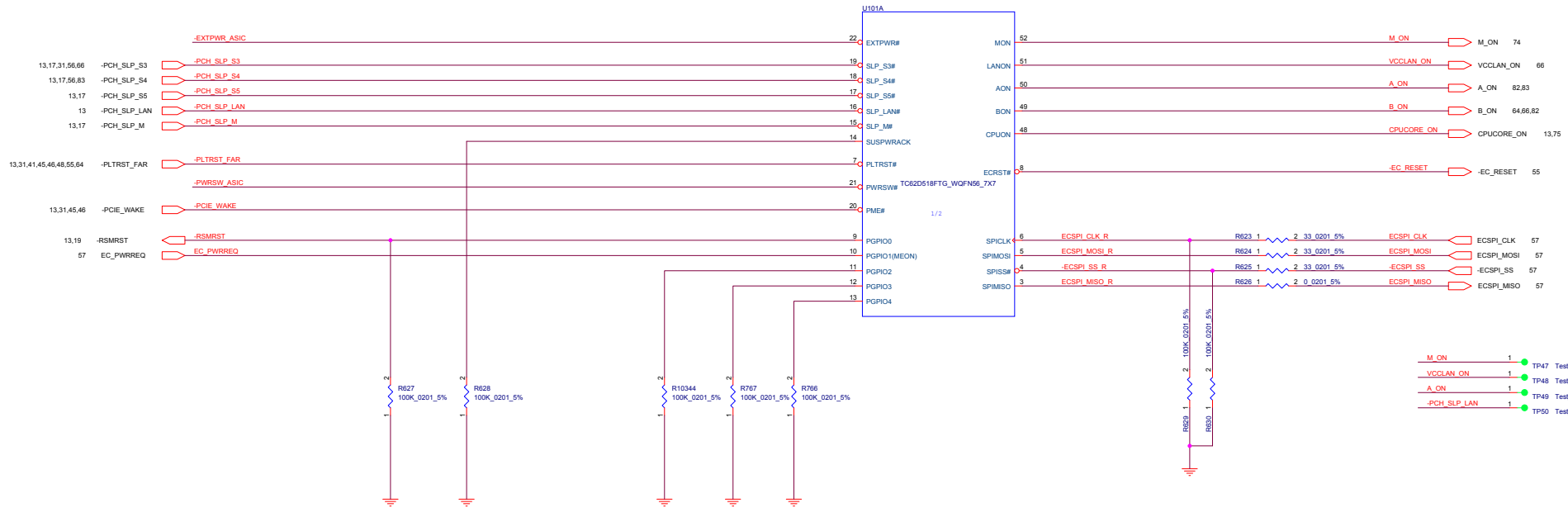
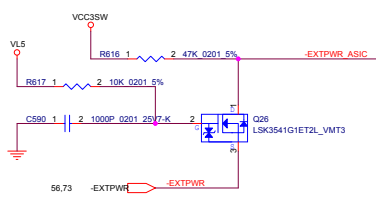
TABLE

REF DES	ENABLE	DISABLE
JLPC	ASM	NO_ASM
R32	ASM	NO_ASM

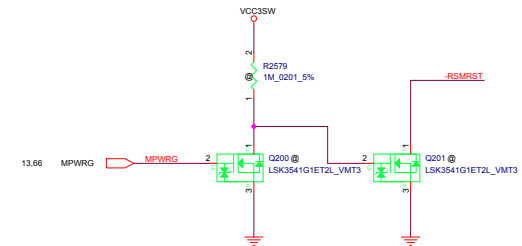
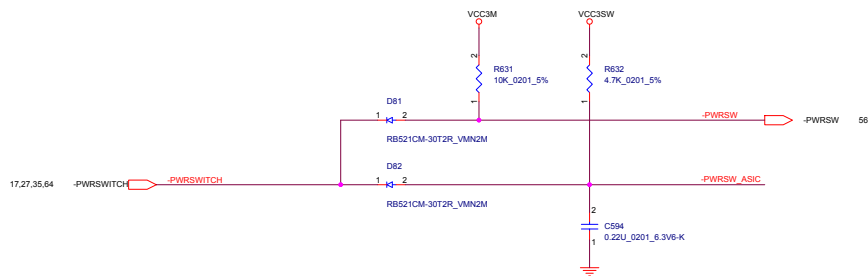
LOGIC

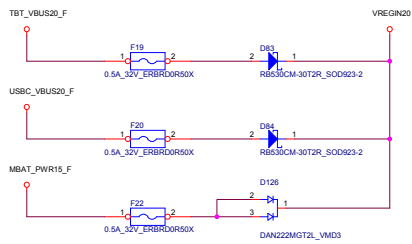






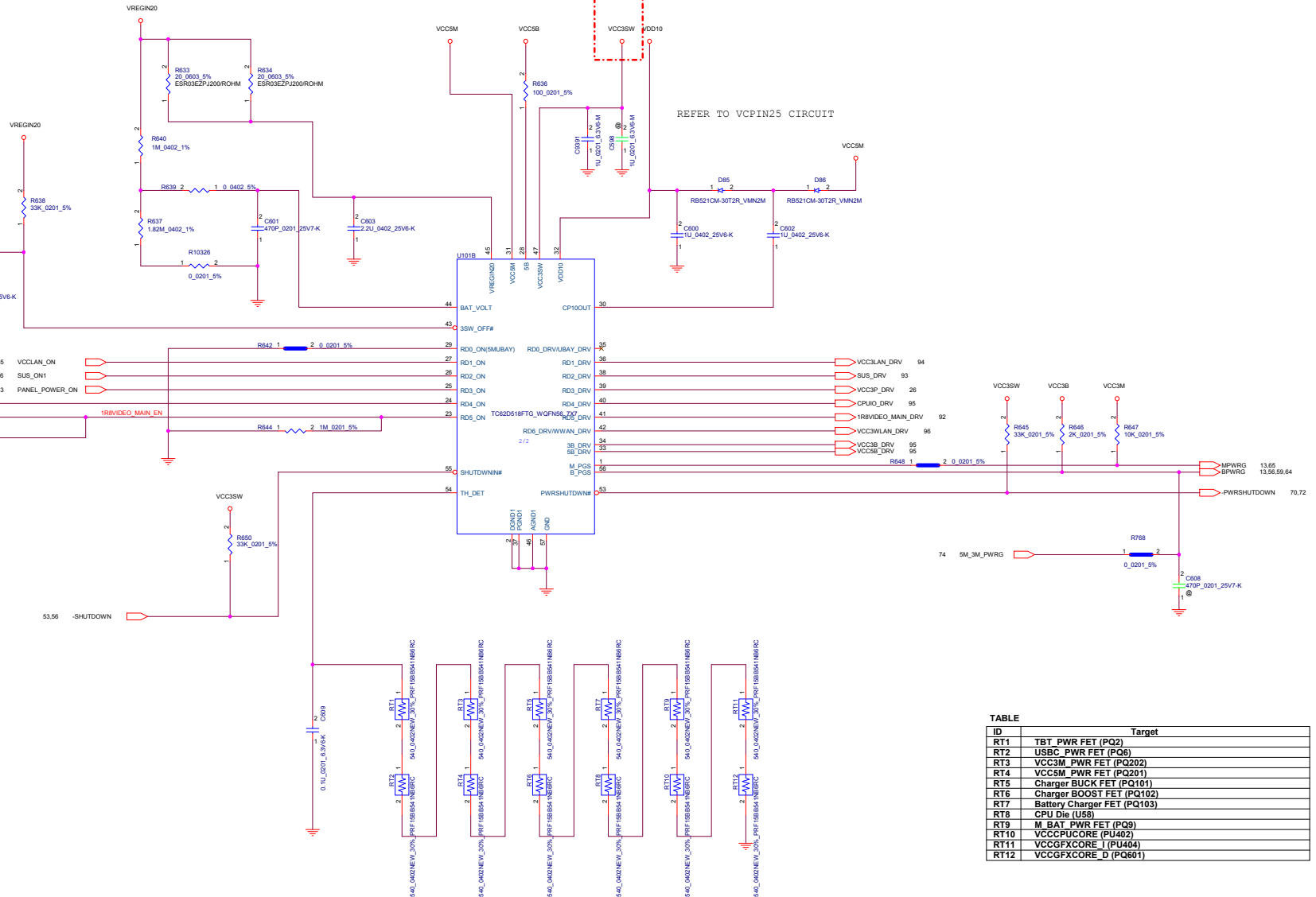
M\_ON 1 TP47 Test\_Point\_20MIL  
 VCCLAN\_ON 1 TP48 Test\_Point\_20MIL  
 A\_ON 1 TP49 Test\_Point\_20MIL  
 -PCH\_SLP\_LAN 1 TP50 Test\_Point\_20MIL





R633, R634 : Need Anti-surge Chip Resistors

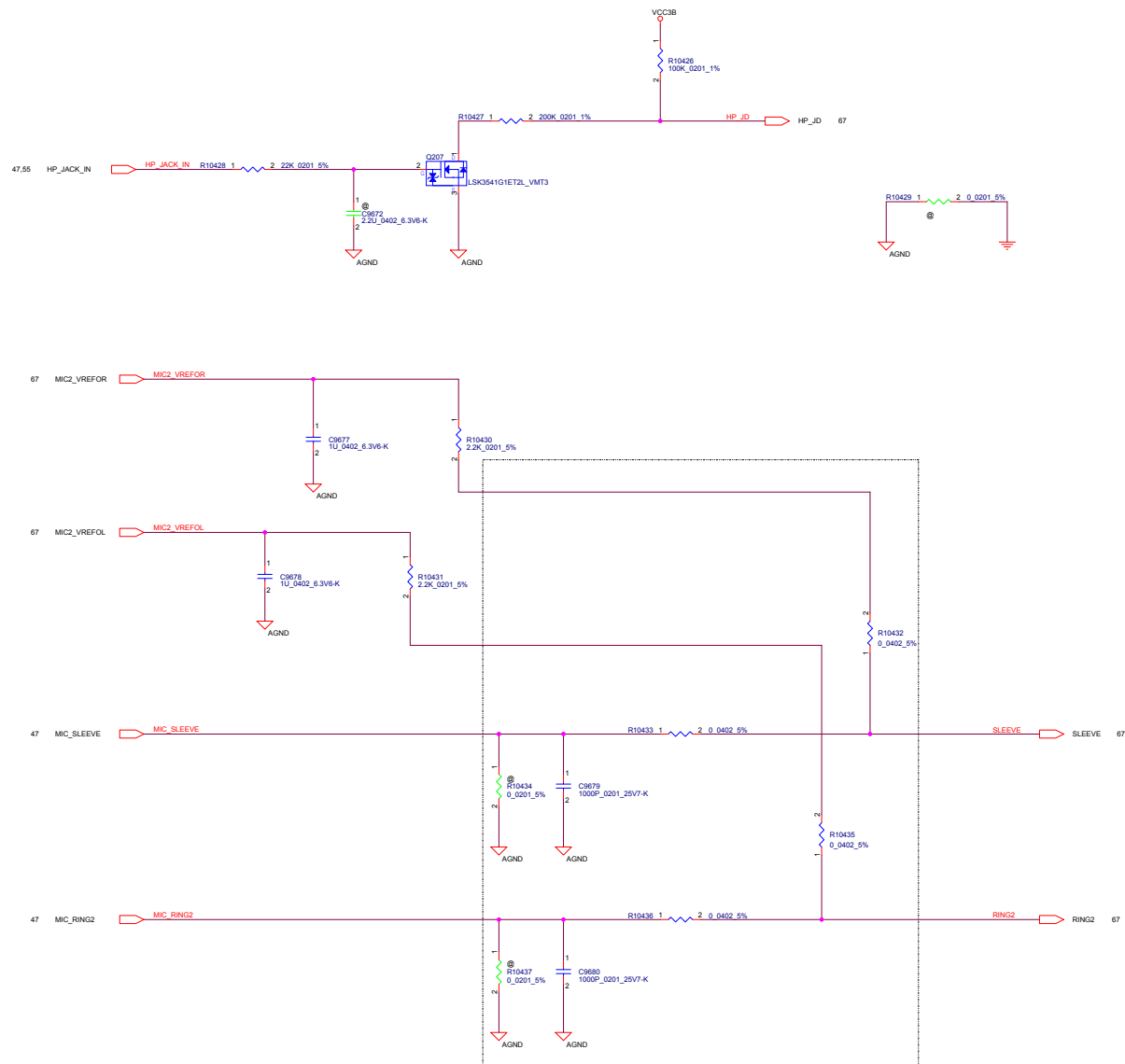
VCC3SW max capacitance: 4.7uF

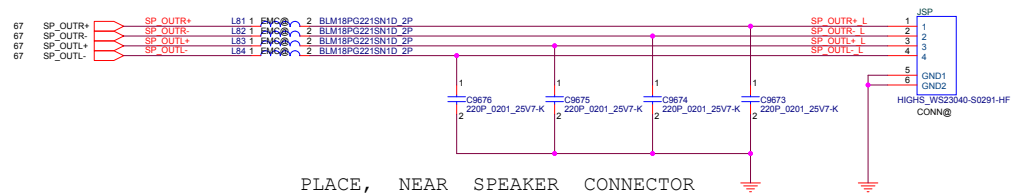


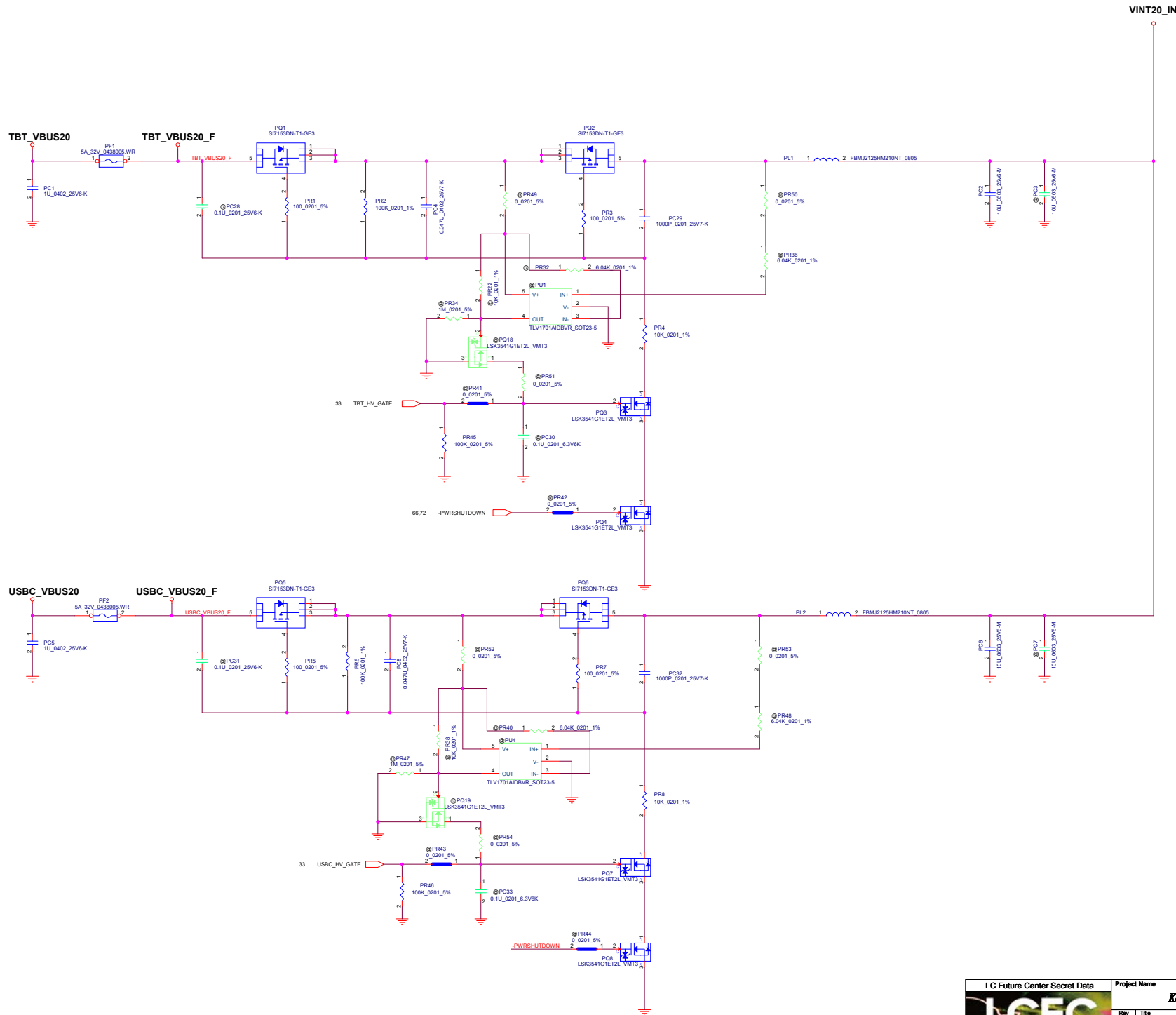
TABLE

ID	Target
RT1	TBT_PWR FET (PQ2)
RT2	USBC_PWR FET (PQ6)
RT3	VCC3M_PWR FET (PQ202)
RT4	VCC5M_PWR FET (PQ201)
RT5	Charger BUCK FET (PQ101)
RT6	Charger BOOST FET (PQ102)
RT7	Battery Charger FET (PQ103)
RT8	CPU Die (USB)
RT9	M_BAT_PWR FET (PQ9)
RT10	VCCCPUCORE (PU402)
RT11	VCCGFXCORE_I (PU404)
RT12	VCCGFXCORE_D (PQ601)

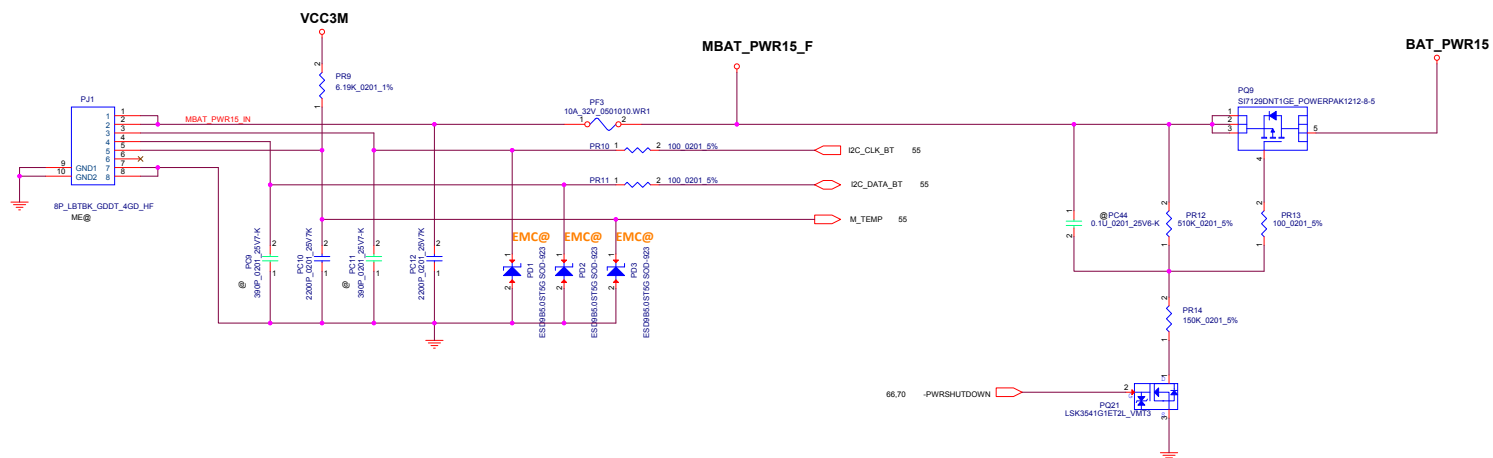






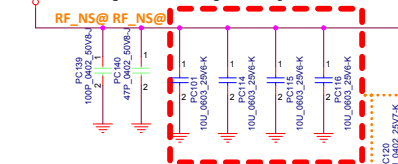


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VINT20\_IN MLCCs must be placed symmetrically on Top and Bottom.



Should be placed near ACP, ACN

Keep these two signals as pair routing

Keep these two signals as pair routing

MLCCs must be placed symmetrically on Top and Bottom.

Table PL101

CYNTEC, CMLE063T-2R2MS-88  
TOKO, FDSD0630-H-2R2M=P3

TABLE:ILIM\_HIZ

IDPM	V(ILIM)	PR123
500mA	1.2V	402K
1.0A	1.4V	332K
1.5A	1.6V	280K
2.0A	1.8V	237K
3.0A	2.2V	174K
3.25A	2.3V	162K

← LOGIC

TABLE

Inductor	R(IADP)	fsw@POR
1.0uH	93kohm	800kHz
1.5uH	108kohm	800kHz
2.2uH	137kohm	800kHz

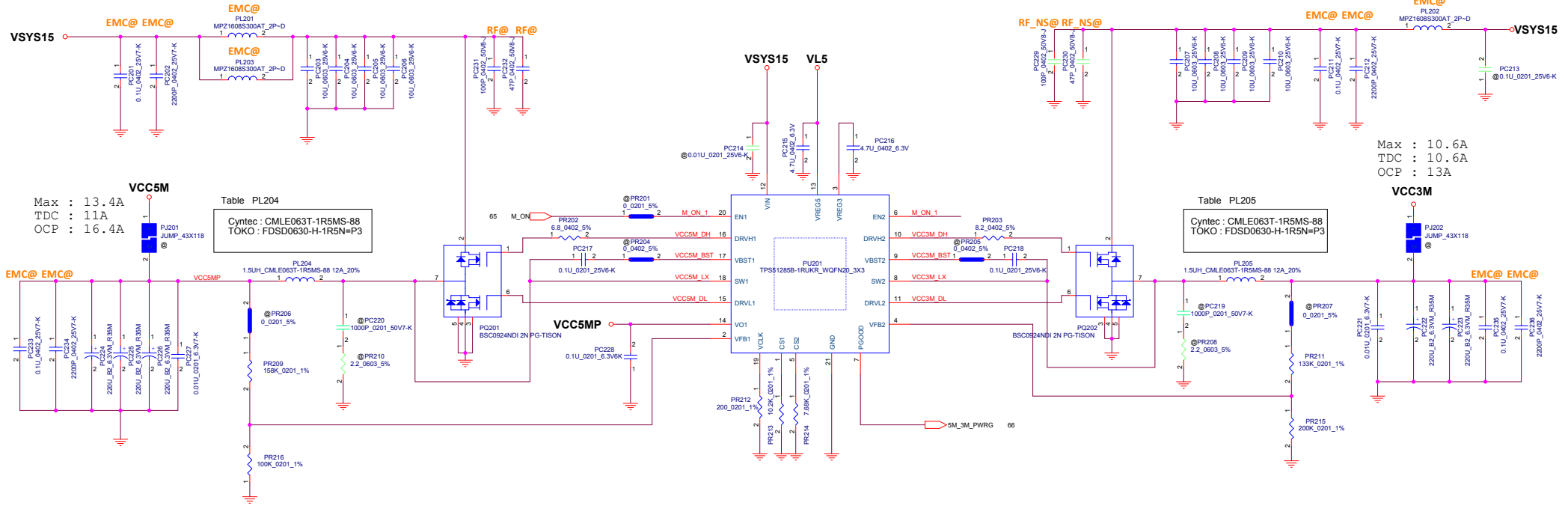
TABLE:CELL\_BATPRES

# of CELL	VCCELL_PRES	PR129
1-CELL	1.5V	301K
2-CELL	2.5V	140K
3-CELL	3.5V	71.5K
4-CELL	4.5V	33.2K

← LOGIC

All the input MLCCs on 15V must be placed symmetrically on Top and Bottom.

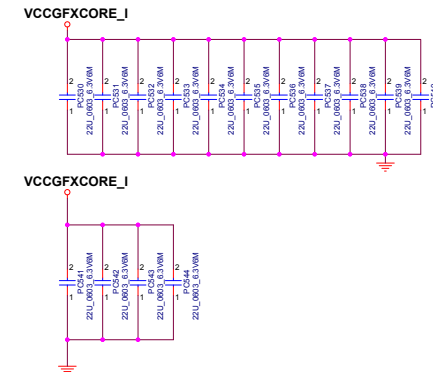
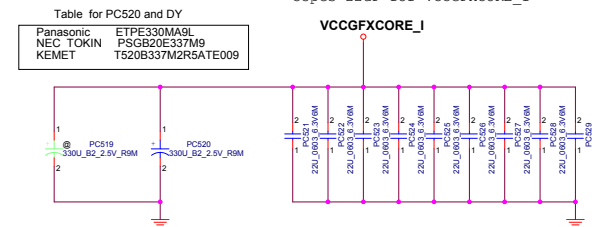
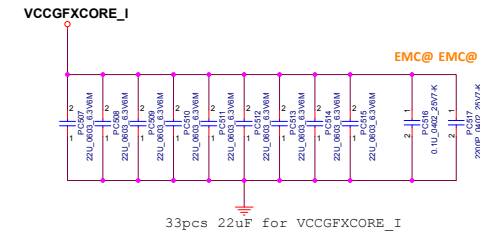
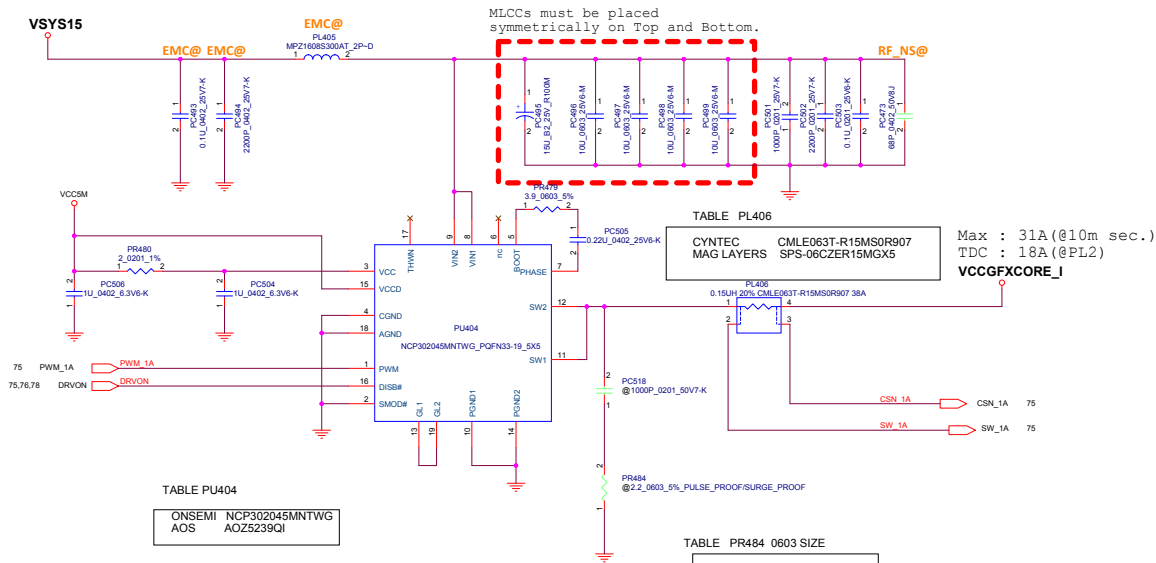
All the input MLCCs on 15V must be placed symmetrically on Top and Bottom.



<div> <div>LCFC</div> <div>LC Future Center Secret Data</div> </div>	Project Name	
	Kolar-1	
	Rev	Title
	4.02	DC/DC VCC5M/VCC3M(TPS51285B-1)
Date: Wednesday, November 01, 2017 15:00:00 74 of 97		

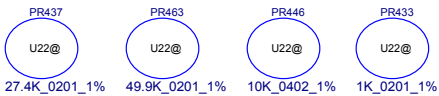









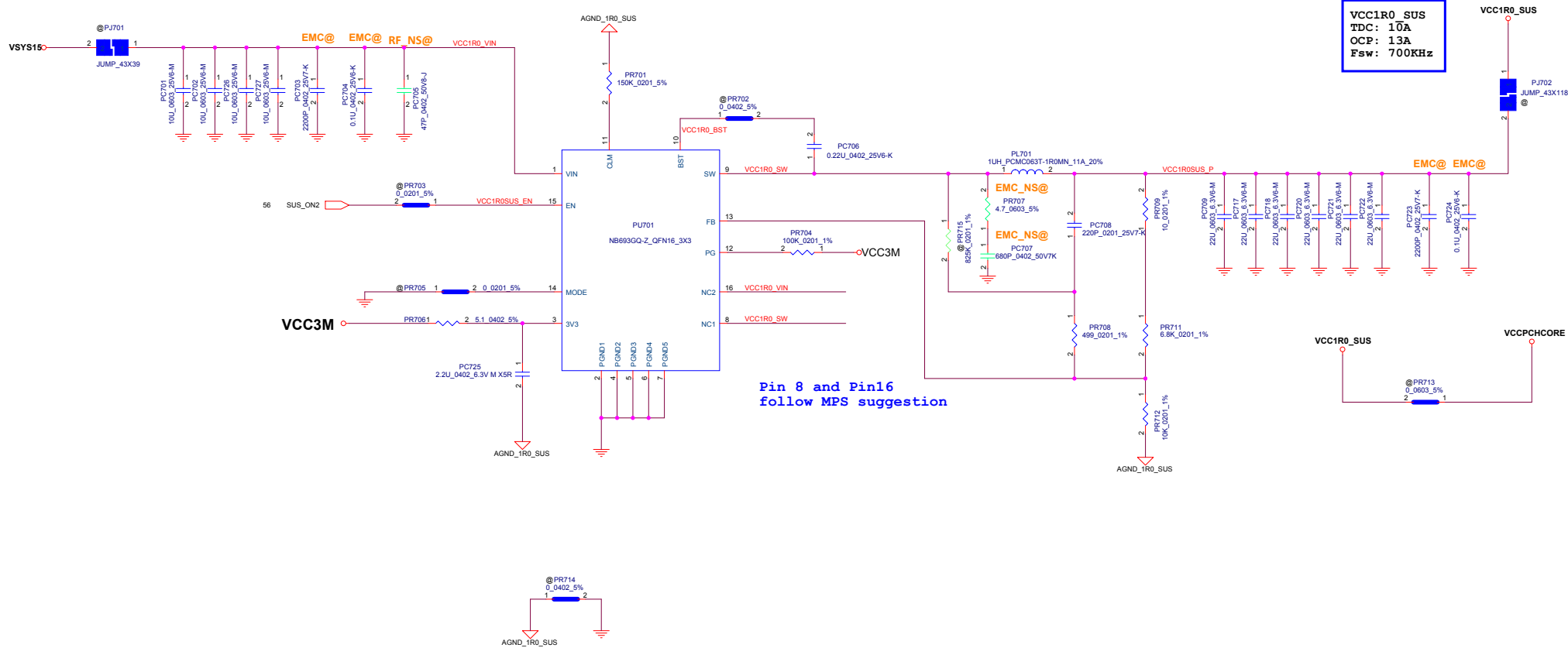
U22 unique

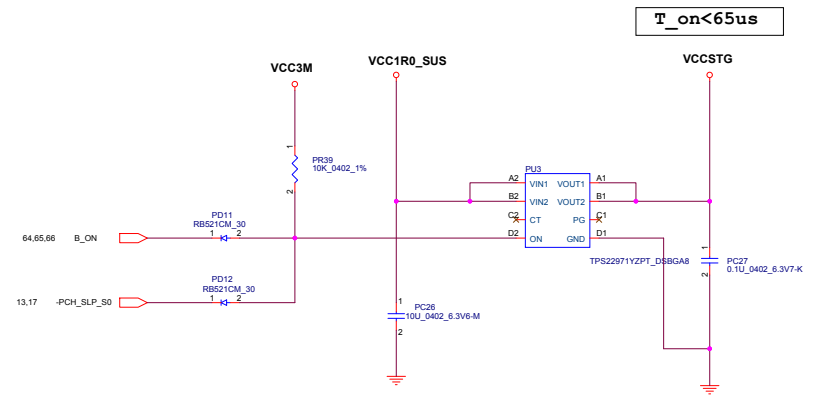
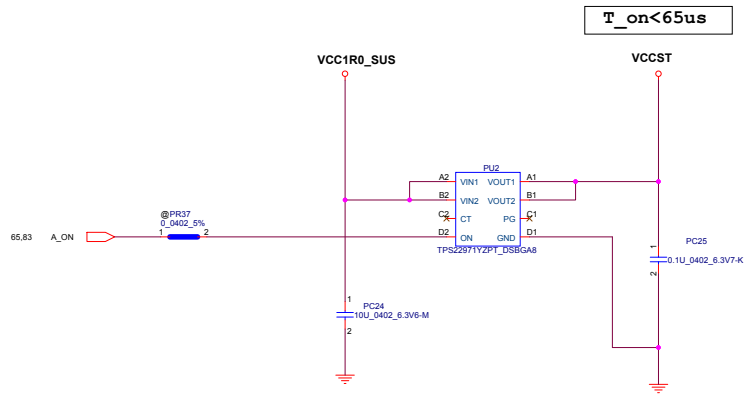


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LC Future Center Secret Data		Project Name	
		<i>Kolar-1</i>	
		Rev 4.02	Title <b>BLANK</b>
Title: Wednesday, November 01, 2017Sheet 80 of 97			







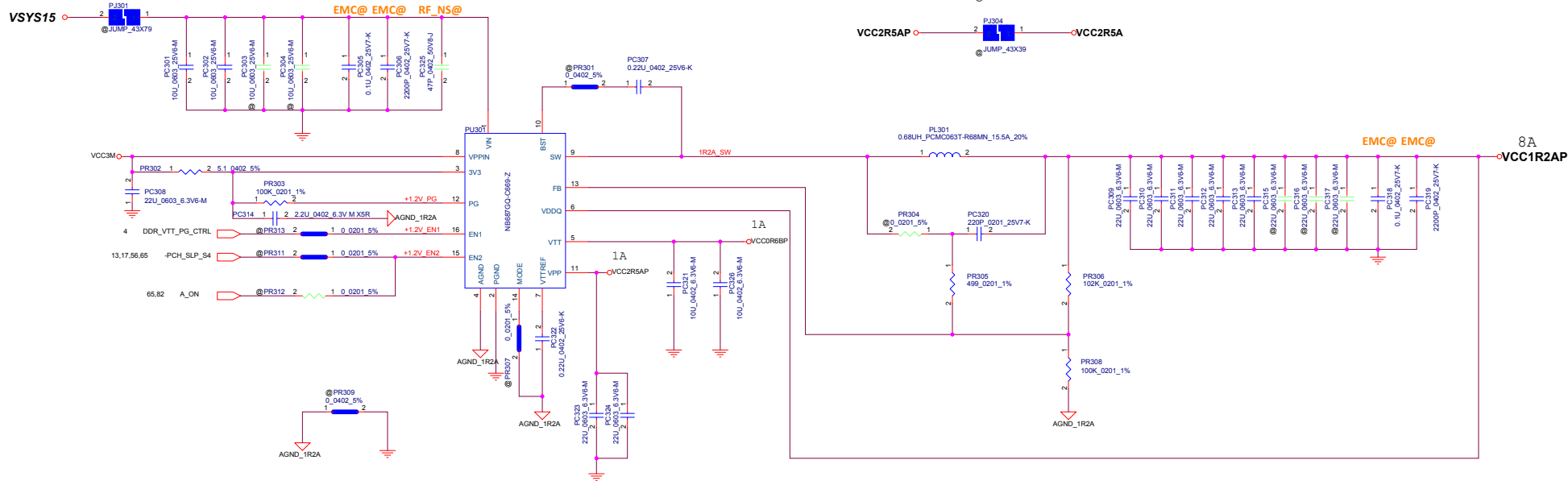



TABLE NB687GQ:EN1/EN2

State	EN1	EN2	VDDQ	VTTREF	VTT	VPP
S0	High	High	ON	ON	ON	ON
S3	Low	High	ON	ON	OFF (High-Z)	ON
S4/S5	Low	Low	OFF	OFF	OFF	OFF
Others	High	Low	OFF	OFF	OFF	OFF

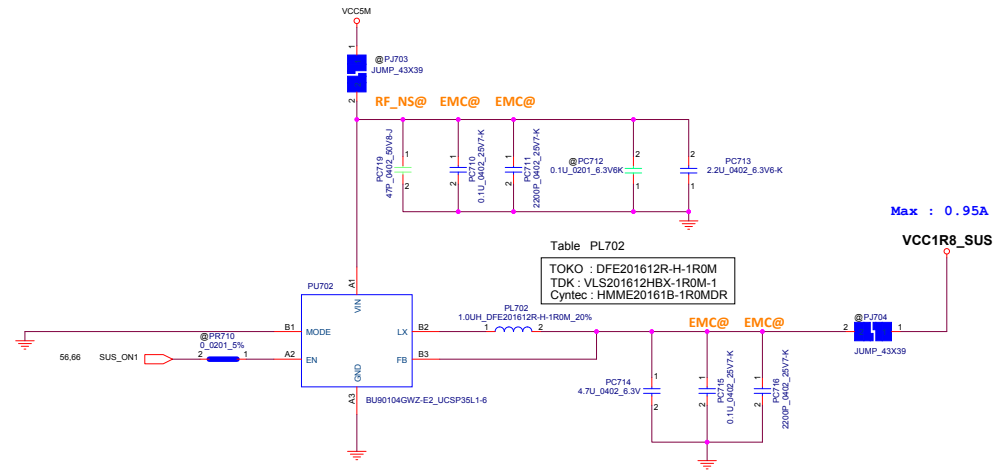
TABLE NB687GQ:MODE

State	USM	Fs	Resistor to GND
M1	NO	700KHz	0
M2	YES	700KHz	90K
M3	NO	500KHz	150K
M4	YES	500KHz	>230K or Float

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LC Future Center Secret Data		Project Name	
		<i>Kolar-1</i>	
		Rev	Title
		4.02	<b>BLANK</b>
Date: Wednesday, November 01, 2017Sheet 84 of 97			

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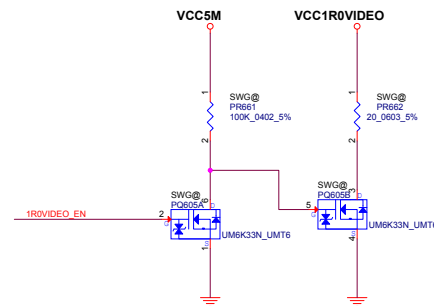
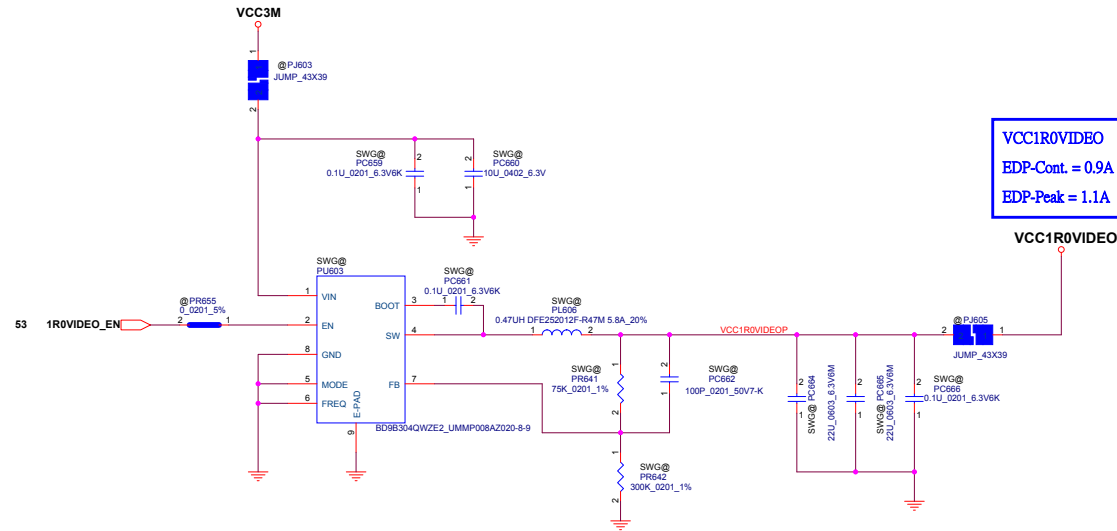


Table PR662 0603 SIZE

Rohm: ESR03EZPJ200  
Pana: ERJP03J200  
KOA: SG73P1JTTD200J

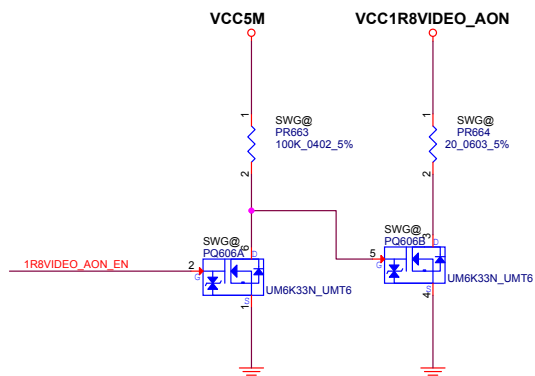
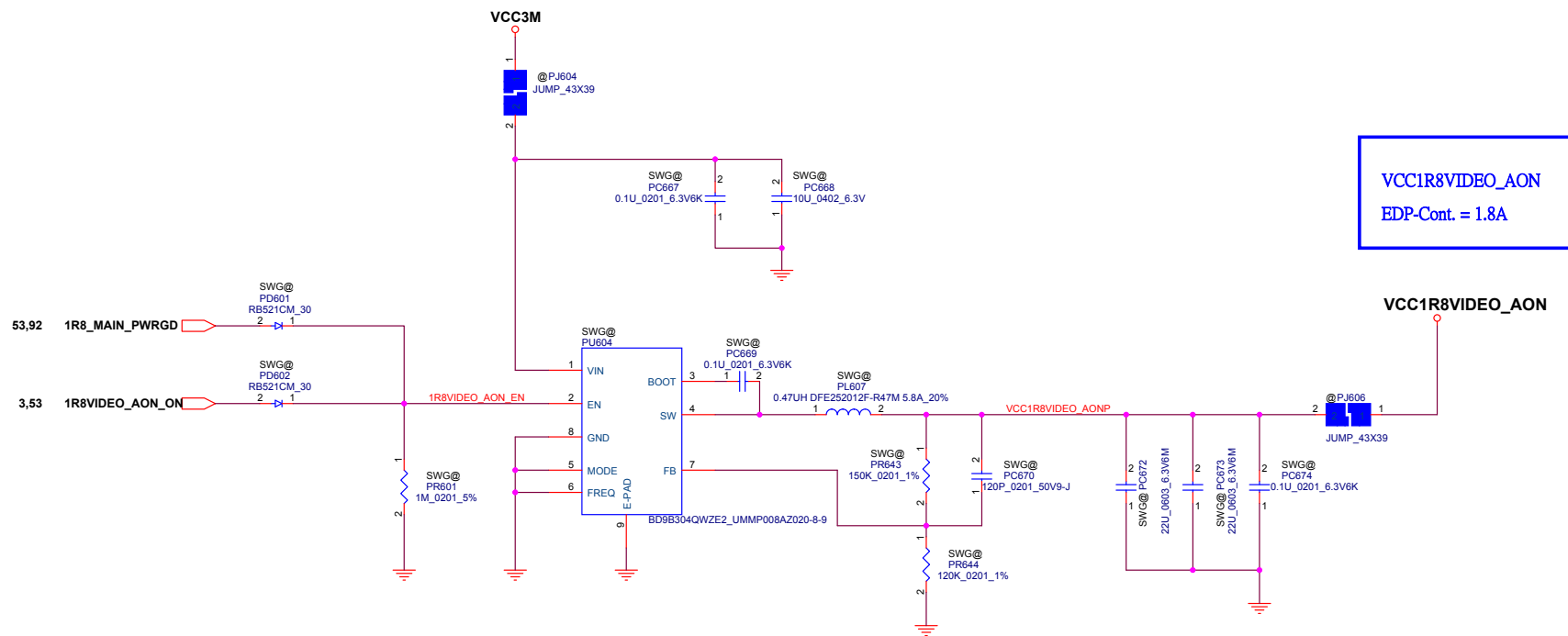


Table PR664 0603 SIZE

Rohm: ESR03EZPJ200  
Pana: ERJP03J200  
KOA: SG73P1JTTD200J

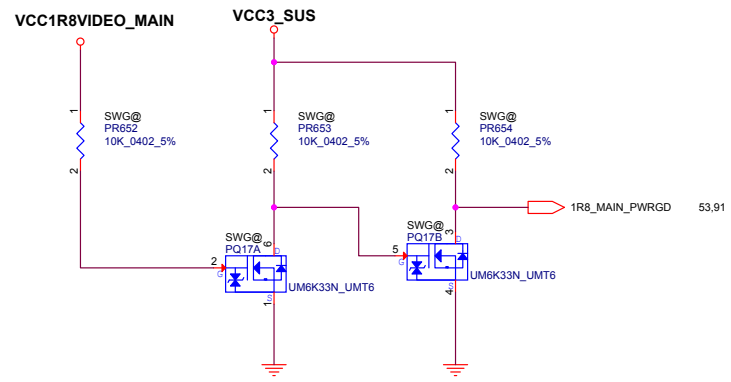
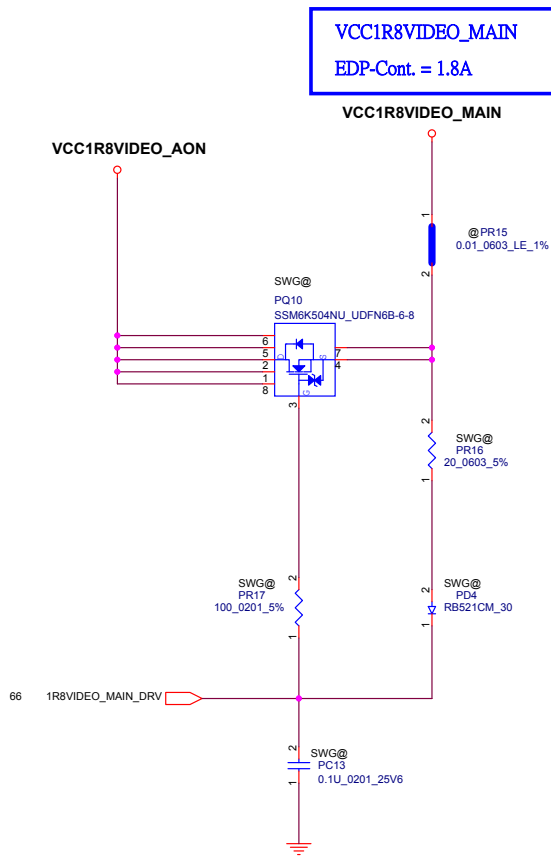


Table PR16 0603 SIZE

Rohm:ESR03EZPJ200  
Pana:ERJP03J200  
KOA:SG73P1JTTD200J

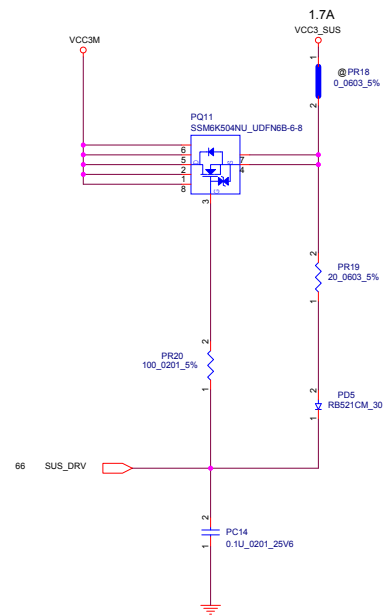


Table PR19 0603 SIZE

Rohm:ESR03EZPJ200  
Pana:ERJP03J200  
KOA:SG73P1JTTD200J

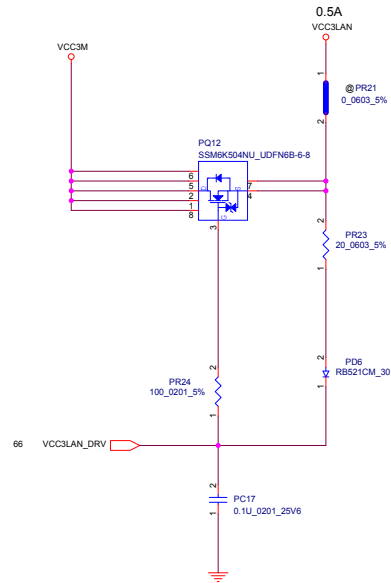
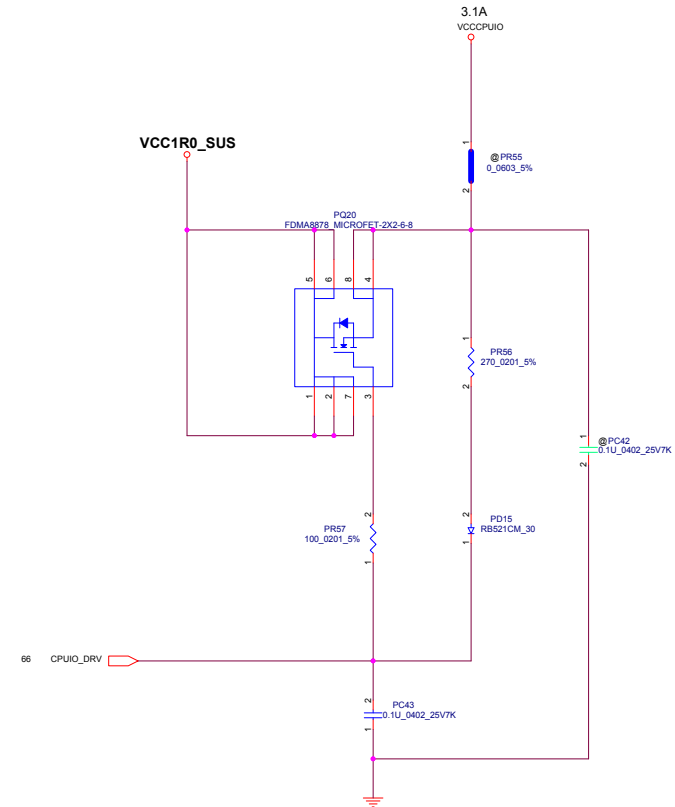
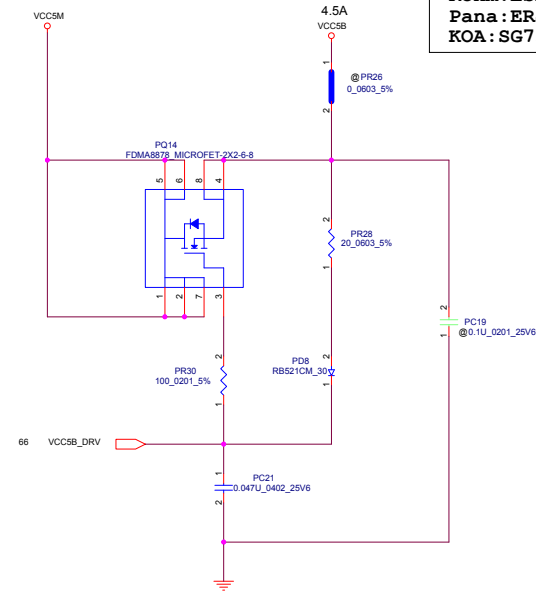
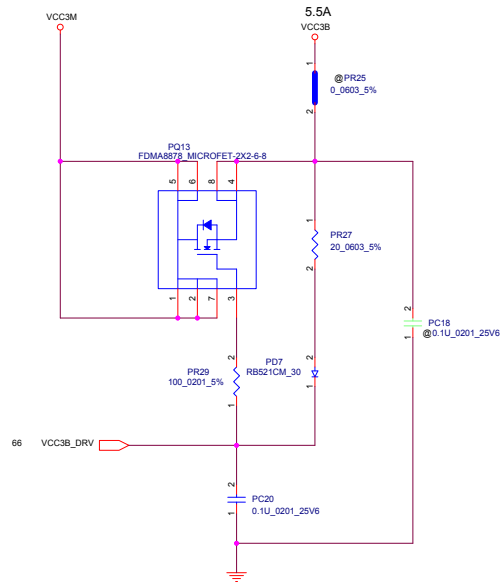


Table PR23 0603 SIZE

Rohm:ESR03EZPJ200  
Pana:ERJP03J200  
KOA:SG73P1JTTD200J

Table PR27,PR28 0603 SIZE

Rohm: ESR03EZPJ200  
Pana: ERJP03J200  
KOA: SG73P1JTTD200J



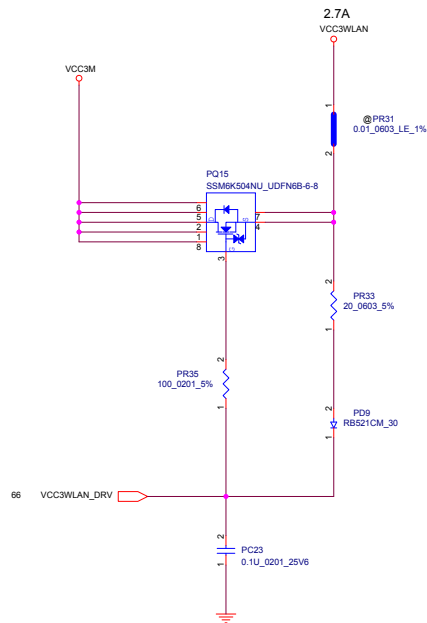
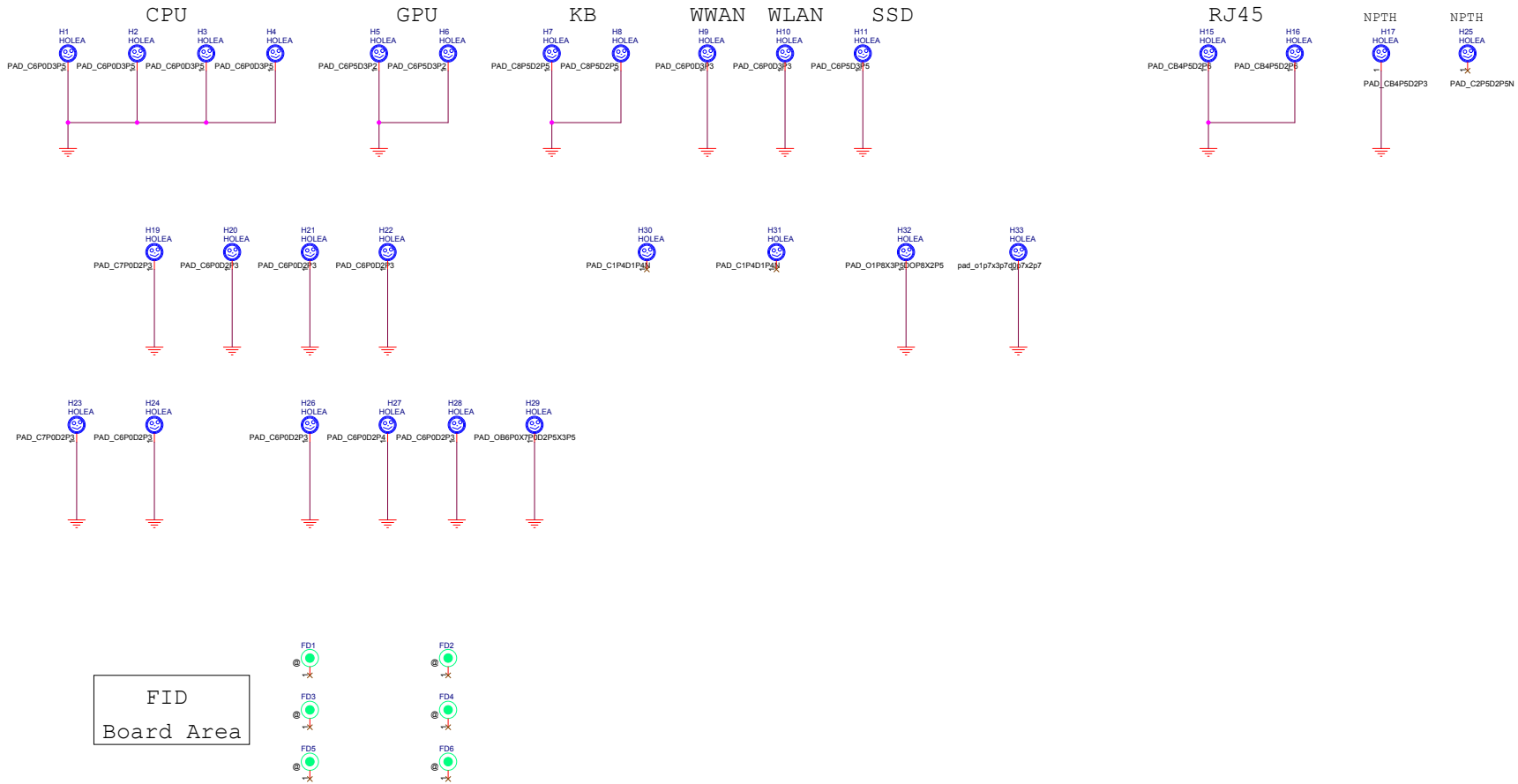
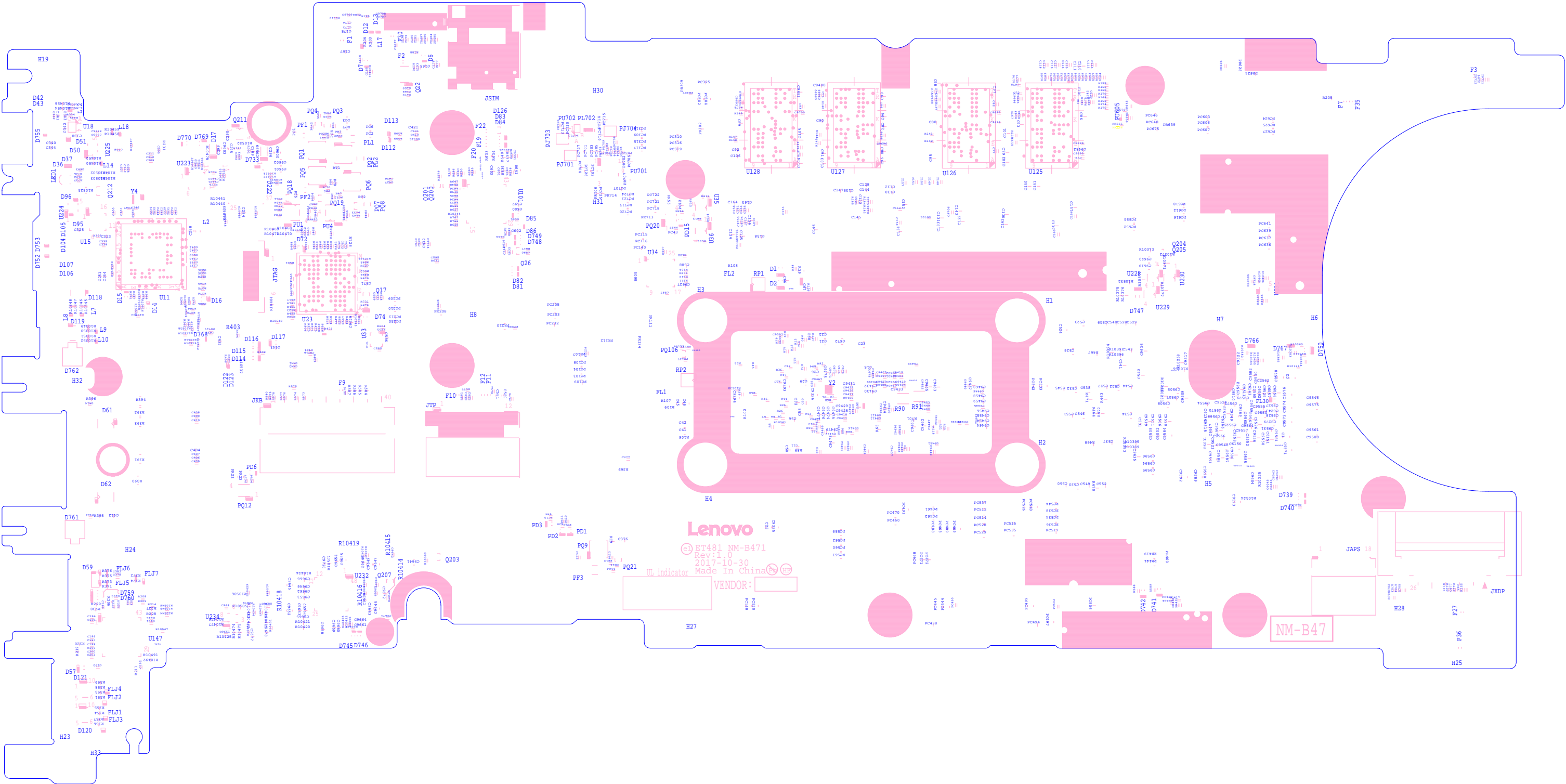


Table PR33 0603 SIZE

Rohm:ESR03EZPJ200  
Pana:ERJP03J200  
KOA:SG73P1JTTD200J







LCFC ELECTRONICS. INC.	
PROJECT	ET481
BOARD NO.	NM-B471 REV:1.0
LAYER NO.	SILKSCREEN_TOP
DRAW BY	JANE
Issued Date	2017-10-30
Security level	Confidential
Decipherment date	2018-10-30



Decipherment date	2018-10-30
Security level	Confidential
Issued Date	2017-10-30
DRAW BY	JANE
LAYER NO.	SILKSCREEN_BOTTOM
BOARD NO.	NM-B471 REV:1.0
PROJECT	ET481
LCFC ELECTRONICS . INC.	